XHFC Series Evaluation Kit

U_{pN} / U_{p0} Port Line Interface Subassembly

Revision 2

Hardware Description

January 2016

Contents

1 Overview

U_p Port Line Interface Subassembly is an ISDN line interface module which is part of to the XHFC Series Evaluation Kit of Cologne Chip. Both TE mode and NT mode can be used with this U_{pN}/ U_{p0} [1] module.

The XHFC Series Evaluation Kit family consists of several evaluation board variants [1, 2, 3] and different line interface subassemblies which have to be piggybacked onto the evaluation boards.

The U_p interface circuitry is intended for use with

- installation cable (e.g. Cat.3 / J-Y(St)Y n×2×0,6) with a signal reach of up to approximately 2 km or
- shielded ground cable with a signal reach of up to approximately 4 km.

> **Please note !**
>
> Please do not consider U_{pN}/ U_{p0} to be identical to U_{k0}.
>
> U_{pN}/ U_{p0} is used in private networks for ISDN data and voice communication via 2 wires, e.g. for terminal equipment such like ISDN phones, to an ISDN PABX. U_{pN}/ U_{p0} uses the time division multiplex method (ping-pong). [4]
>
> U_{k0} is utilized for the last mile from central office to the local subscriber. 2-wire full-duplex with echo cancelling (2B1Q or 4B3T line code) is used. U_{k0} is not supported by XHFC series microchips.

2 Module description

The U_p interface circuitry shown in Figure 1 on page 3 is qualified for both TE mode and NT mode.

> **Please note !**
>
> In contrast to the board design of the XHFC Series Evaluation Kit, C1 and C2 should be located as near as possible to the XHFC series microchip pins L_A and L_B.
>
> R1 . . R4 should be located near to the XHFC series microchip pins as well.
>
> If chassis ground is available C10 . . C12 should be added to improve EMI characteristics.
>
> In this respect, the XHFC Series Evaluation Kit should not be taken as an example for product development.

Pins 5 and 7 of connector CON1 are reserved for service bits (GPIO). They are not used on the U_p Port Line Interface Subassembly. Thus, these GPIO signals are not needed on the XHFC evaluation board with this subassembly used.

Views of the board design are shown in Figures 2 to 5 from page 5.

[1] U_{pN}/ U_{p0} in the following referred to as U_p.

3 Module schematic

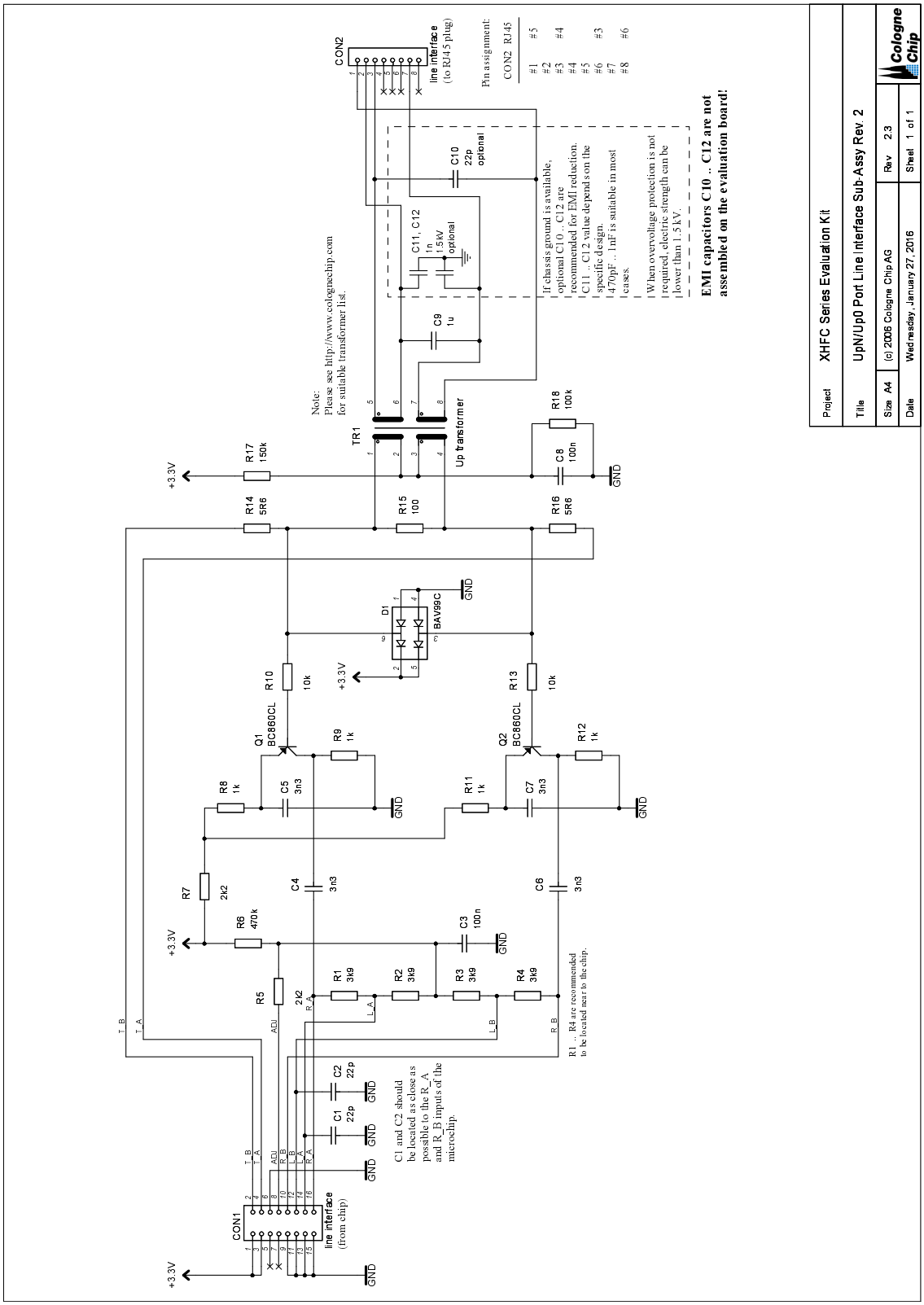

Figure 1: *U_P Port Line Interface Subassembly*

Bill of Materials: **XHFC Series Evaluation Kit**

UpN/Up0 Port Line Interface Sub-Assy Rev. 2

Revision: 2.3, generated on Wednesday, January 27, 2016 by Cologne Chip AG

Resistors (18 pcs.)

R1,R2,R3,R4	3k9
R5,R7	2k2
R6	470k
R8,R9,R11,R12	1k
R10,R13	10k
R14,R16	5R6
R15	100
R17	150k
R18	100k

Capacitors 9 pcs.)

C1,C2	22p
C3,C8	100n
C4,C5,C6,C7	3n3
C9	1u
C10	22p
C11,C12	1n, 1.5kV

Diodes (1 pc.)

D1	BAV99C

Transistors (2 pcs.)

Q1,Q2	BC860CL

Transformers (1 pc.)

TR1	Up transformer

Connectors (2 pcs.)

CON1	CON2X8
CON2	CON1X8

Total:

18 x Resistors
12 x Capacitors
1 x Diodes
2 x Transistors
1 x Transformers
2 x Connectors

36 total

Note:

If chassis ground is available, optional C10 .. C12 are recommended for EMI reduction.

C11 .. C12 value depends on the specific design. 470pF .. 1nF is suitable in most cases.

When overvoltage protection is not required, electric strength can be lower than 1.5 kV.

4 Module layout

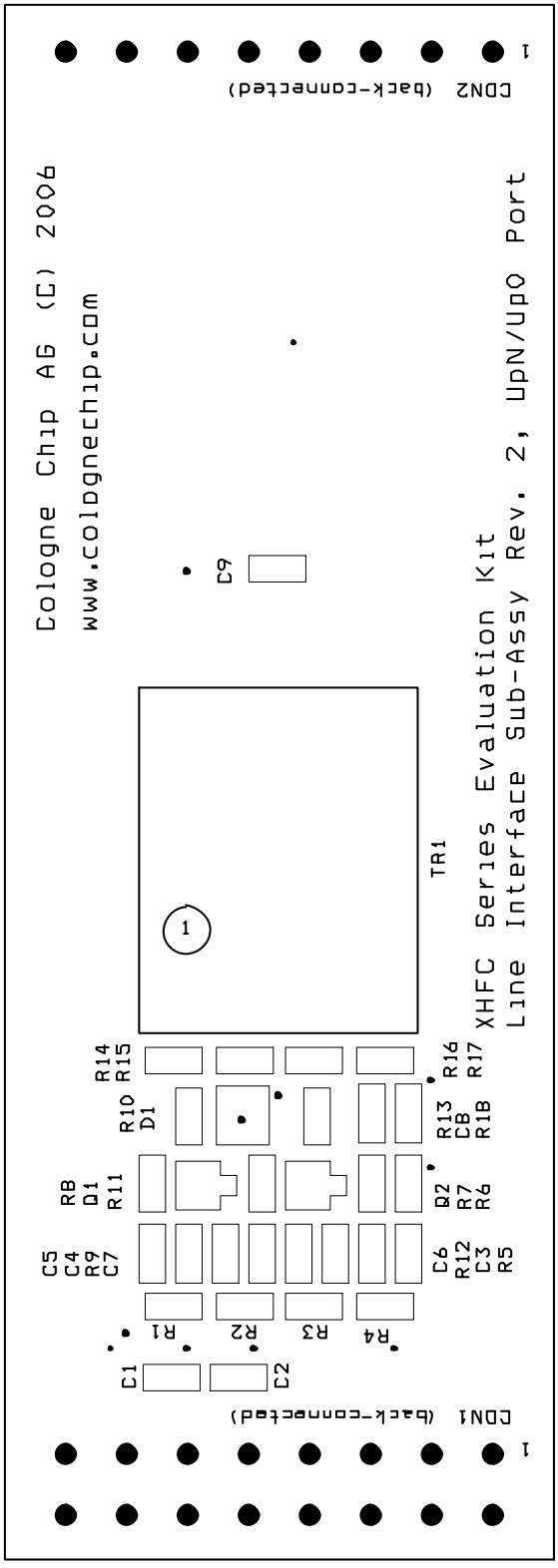

Figure 2: *U_p Port Line Interface Subassembly board (top side inscription)*

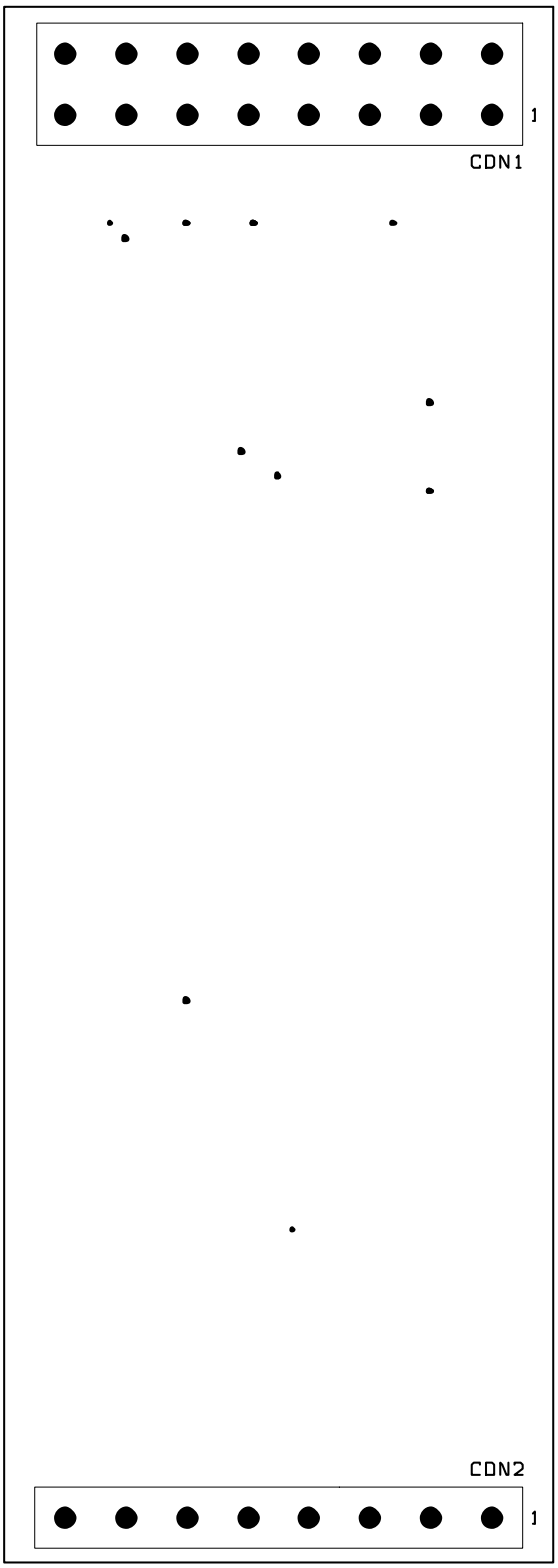

Figure 3: *U_p Port Line Interface Subassembly board (bottom side inscription)*

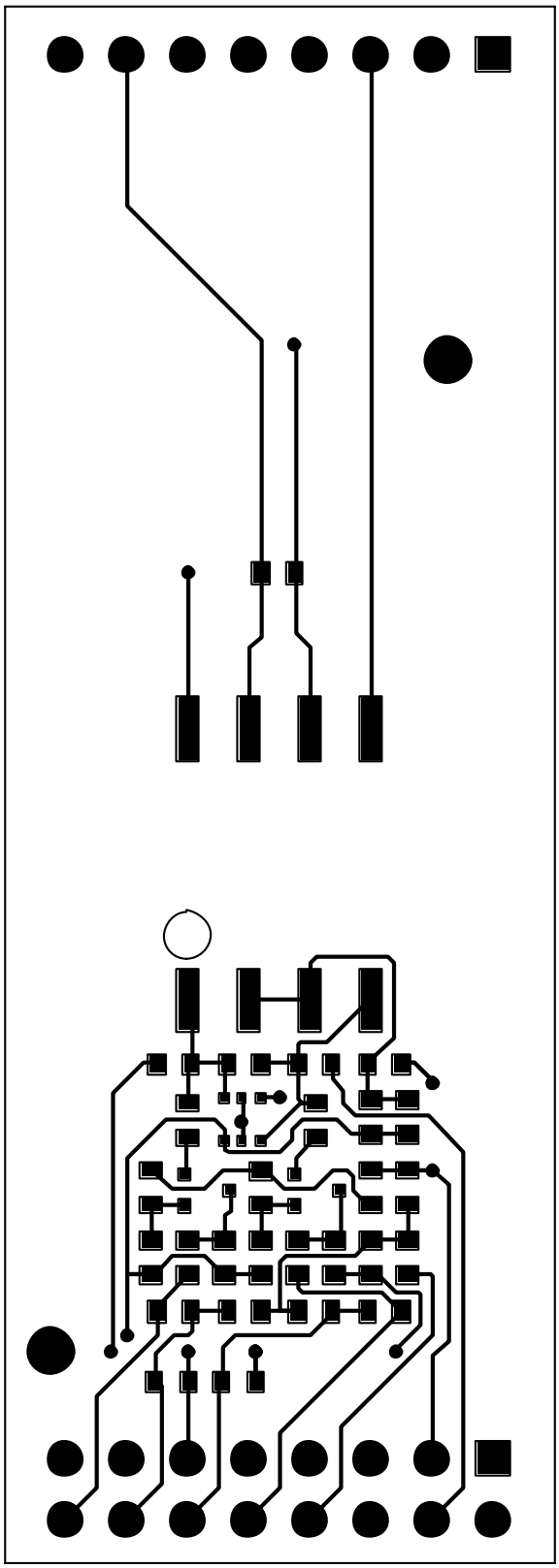

Figure 4: *U_p Port Line Interface Subassembly board (top side traces)*

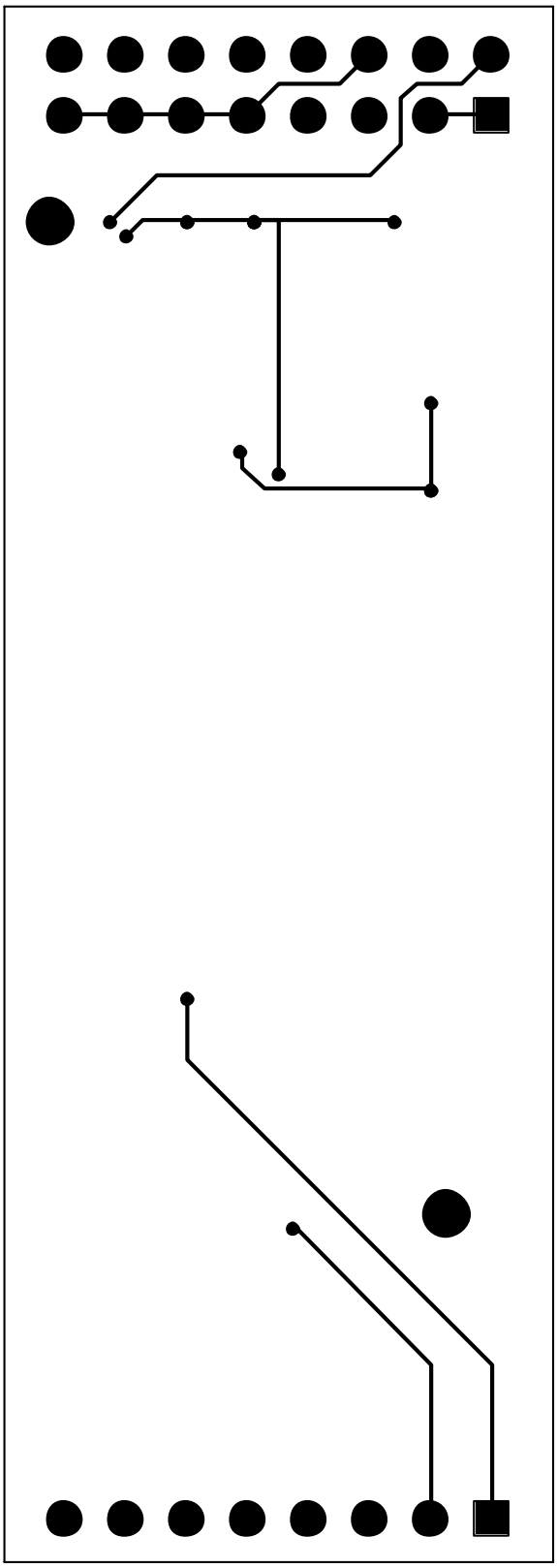

Figure 5: *U_p Port Line Interface Subassembly board (bottom side traces)*

References

[1] Cologne Chip AG. *XHFC Series Evaluation Kit. XHFC - 1SU Evaluation Board Rev. 1*, January 2016.

[2] Cologne Chip AG. *XHFC Series Evaluation Kit. XHFC - 2SU Evaluation Board Rev. 1*, January 2016.

[3] Cologne Chip AG. *XHFC Series Evaluation Kit. XHFC - 4SU Evaluation Board Rev. 1*, January 2016.

[4] Electronic Manufacturing Industry Association of Germany, Information & Communication Technology Group (ZVEI Zentralverband Elektrotechnik, Fachverband Informations- und Kommunikationstechnik (I+K Forum)). *ZVEI Documentation DKZ-N; Interfaces and signaling protocols for ISDN telecommunication installations. (only available in German under title: ZVEI-Dokumentation DKZ-N; Schnittstellen und Signalisierungsprotokolle für Telekommunikationsanlagen im ISDN)*, Mai 1989. Volume IV: DKZ-N part 1.2, DKZ-N2 part 2.2.