Cologne Chip

# XHFC Series Evaluation Kit

## ST / $U_p$ Port Line Interface Subassembly with Coding Plug

## Revision 1

## Hardware Description

**Cologne Chip AG**
**Eintrachtstrasse 113**
**D - 50668 Köln**
**Germany**

**Tel.: +49 (0) 221 / 91 24-0**
**Fax: +49 (0) 221 / 91 24-100**

**http://www.CologneChip.com**
**http://www.CologneChip.de**
**support@CologneChip.com**

# Contents

# 1 Overview

The S/T Port Line Interface Subassembly with Coding Plug is an ISDN line interface module which is part of the XHFC Series Evaluation Kit of Cologne Chip. This module can be used for either S/T or $U_p$ line interface mode [1]. Further, TE or NT mode can be selected, power feeding can be switched on or off and line termination can also be enabled or disabled. All these feature selections are accomplished by dedicated coding plugs.

The XHFC Series Evaluation Kit family consists of several evaluation board variants [1, 2, 3] and different line interface subassemblies which have to be piggybacked onto the evaluation boards.

**Please note !**

Please do not consider $U_{pN}$/ $U_{p0}$ to be identical to $U_{k0}$.

$U_{pN}$/ $U_{p0}$ is used in private networks for ISDN data and voice communication via 2 wires, e.g. for terminal equipment such like ISDN phones, to an ISDN PABX. $U_{pN}$/ $U_{p0}$ uses the time division multiplex method (ping-pong).

$U_{k0}$ is utilized for the trunk line from Central Office to the local subscriber. 2-wire full-duplex with echo cancellation (2B1Q or 4B3T line code) is used. $U_{k0}$ is not supported by XHFC series microchips.

[1] $U_{pN}$/ $U_{p0}$ in the following referred to as $U_p$.

# 2 Module description

A late choice of the line interface mode is an important feature in many applications, such as PABX line cards.

In practice, the electronic technician at the end user's site would like to decide about the interface mode and its configuration. As an example, he could configure an ISDN port in a PABX for trunking to the Central Office (S/T bus, TE mode, not terminated) or he could connect a digital system phone via 2-wire cabling to the same ISDN port ($U_p$ line, NT mode, terminated).

For a cost-effective mass production, only one PCB should offer all possibilities.

A convenient and low-cost solution is shown with the S/T Port Line Interface Subassembly with Coding Plug. The interface mode selection and configuration can be achieved by simple, low-cost coding plugs. These are plugged by the electronic technician. Compared with a set of two-pin jumpers, whose assembly is error-prone, coding plug insertion is fast and mistake-proof. Moreover, the form factor is smaller than a set of jumpers.

The line interface circuitry is shown in Figure 1 on page 6. Four different coding plug options are shown in Figures 2 . . 5 from page 8. Table 1 gives an overview of the here described coding plugs.

**Table 1:** *Coding plug examples*

| Plug No. | Application | Power feeding | Line termination |
|---|---|---|---|
| 1 | S/T interface, TE mode | no | no |
| 2 | S/T interface, NT mode | yes | yes (optional) |
| 3 | $U_p$ interface, NT mode | yes | yes (mandatory) |
| 4 | $U_p$ interface, TE mode | no | yes (mandatory) |

# 3 Module schematic

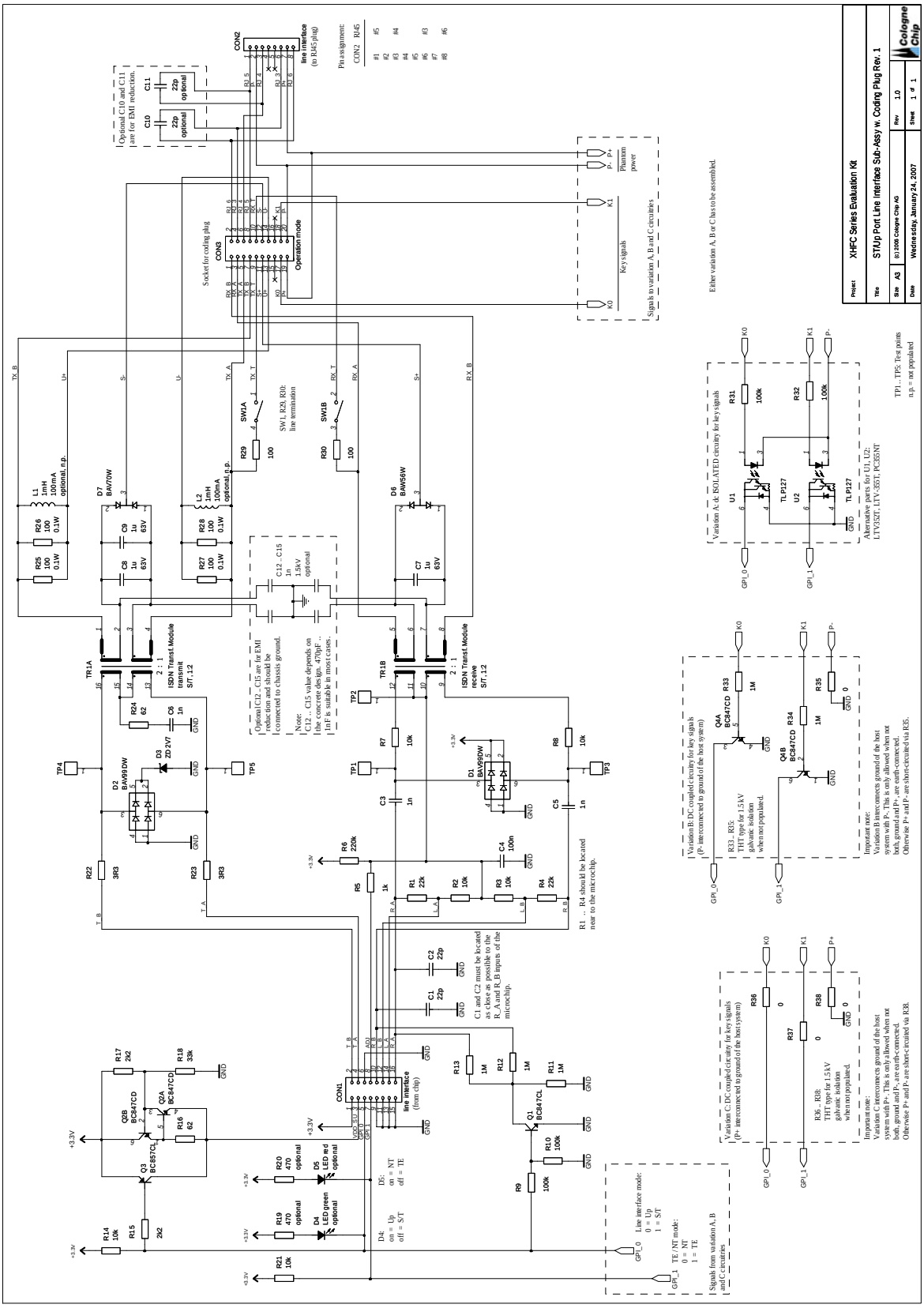


**Figure 1:** *Line Interface Sub-Assy for ST / $U_p$ Port with coding plug*

**Bill of Materials:** **XHFC Series Evaluation Kit**

**ST/Up Port Line Interface Sub-Assy w. Coding Plug Rev. 1**

Revision: 1.0, generated on Wednesday, January 24, 2007 by Cologne Chip AG

(n.p. = not populated)

**Resistors** (28 / 38 pcs.)

| | | |
|---|---|---|
| R1,R4 | 22k | |
| R2,R3,R7,R8,R14,R21 | 10k | |
| R5 | 1k | |
| R6 | 220k | |
| R9,R10 | 100k | |
| R11,R12,R13 | 1M | |
| R15,R17 | 2k2 | |
| R16,R24 | 62 | |
| R18 | 33k | |
| R19,R20 | 470 | optional |
| R22,R23 | 3R3 | |
| R25,R26,R27,R28 | 100 | 0.1W |
| R29,R30 | 100 | |
| R31,R32 | 100k | Variation A |
| R33,R34 | 1M | Variation B |
| R35 | 0 | Variation B |
| R36,R37,R38 | 0 | Variation C |

**Capacitors** (9 / 11 pcs.)

| | | |
|---|---|---|
| C1,C2 | 22p | |
| C3,C5,C6 | 1n | |
| C4 | 100n | |
| C7,C8,C9 | 1u | 63V |
| C10,C11 | 22p | optional |

**Coils/Inductors/Filters** (0 / 2 pcs.)

| | | |
|---|---|---|
| L1,L2 | 1mH | 100mA, optional, n.p. |

**Diodes** (5 / 7 pcs.)

| | | |
|---|---|---|
| D1,D2 | BAV99DW | |
| D3 | ZD 2V7 | |
| D4 | LED green | optional |
| D5 | LED red | optional |
| D6 | BAW56W | |
| D7 | BAV70W | |

**Transistors** (3 / 4 pcs.)

| | | |
|---|---|---|
| Q1 | BC847CL | |
| Q2 | BC847CD | |
| Q3 | BC857CL | |
| Q4 | BC847CD | Variation B |

**Integrated Circuits (ICs)** (0 / 2 pcs.)

| | | |
|---|---|---|
| U1,U2 | TLP127 | Variation A |

**Transformers** (1 pc.)

| | | |
|---|---|---|
| TR1 | ISDN Transf. Module | S/T, 1:2 |

**Switches** (1 pc.)

| | |
|---|---|
| SW1 | Dual switch |

**Connectors** (3 pcs.)

| | |
|---|---|
| CON1 | Female header 2x8 |
| CON2 | Female header 1x8 |
| CON3 | STL21-54CS 2x10 |

**Test Points** (0 / 5 pcs.)

| | | |
|---|---|---|
| TP1,TP2,TP3,-TP4,TP5 | Pin header 1x1 | optional, n.p. |

**Total:**

28 x Resistors
9 x Capacitors
0 x Coils/Inductors/Filters
5 x Diodes
3 x Transistors
0 x Integrated Circuits (ICs)
1 x Transformers
1 x Switches
3 x Connectors
0 x Test Points

| | |
|---|---|
| 50 | total |
| +6 | optional |
| +7 | optional, n.p. |
| +4 | Variation A |
| +4 | Variation B |
| +3 | Variation C |

CON4 is used as a coding plug to select a certain operation mode of the line interface. It must be plugged into connector CON3 of the "ST/Up Port Line Interface Sub-Assy with Coding Plug".

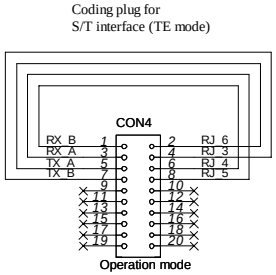


**Figure 2:** *Coding plug No. 1*

| | S/T interface (TE mode): |
|---|---|
| TX / RX signals: | RX_B - RJ_4: #1 - #6<br>RX_A - RJ_5: #3 - #8<br>TX_A - RJ_6: #5 - #2<br>TX_B - RJ_3: #7 - #4 |
| Power feeding: | S+, S- (#11, #12) unconnected<br>(no power feeding) |
| Line termination: | TX_T, RX_T (#9, #10) unconnected<br>(no termination) |
| Key signals: | GPI_0 = 1 / GPI_1 = 1<br>K0, K1 (#17, #18) unconnected |

CON4 pins 15 and 16 are not connected for 1.5 kV galvanic isolation.

The host processor can detect the used coding plug via GPI_0, GPI_1 signals (derived from key signals K0, K1).

| | | | |
|---|---|---|---|
| Project | XHFC Series Evaluation Kit | | |
| Title | Coding Plug No. 1 for S/T interface in TE mode (Rev. 1) | | |
| Size A4 | (c) 2006 Cologne Chip AG | Rev 1.0 | Cologne Chip |
| Date | Friday, January 26, 2007 | Sheet 1 of 1 | |

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CON4 is used as a coding plug to select a certain operation mode of the line interface. It must be plugged into connector CON3 of the "ST/Up Port Line Interface Sub-Assy with Coding Plug".

Coding plug for
S/T interface (NT mode)




| | S/T interface (NT mode): |
|---|---|
| TX / RX signals: | RX_B - RJ_3: #1 - #4<br>RX_A - RJ_6: #3 - #2<br>TX_A - RJ_5: #5 - #8<br>TX_B - RJ_4: #7 - #6 |
| Power feeding: | S+: #11-#19<br>S-: #12-#20 |
| Line termination: | TX: #9-#7<br>RX: #10-#1 |
| Key signals: | GPI_0 = 1 / GPI_1 = 0<br>K0 (#17) unconnected<br>K1 - P+: #18 - #19 |

CON4 pins 15 and 16 are not connected for 1.5 kV galvanic isolation.

The host processor can detect the used coding plug via GPI_0, GPI_1 signals (derived from key signals K0, K1).

| | | | |
|---|---|---|---|
| Project | XHFC Series Evaluation Kit | | |
| Title | Coding Plug No. 2 for S/T interface in NT mode (Rev. 1) | | |
| Size A4 | (c) 2006 Cologne Chip AG | Rev 1.0 | Cologne Chip |
| Date | Friday, January 26, 2007 | Sheet 1 of 1 | |

**Figure 3:** *Coding plug No. 2*

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CON4 is used as a coding plug to select a certain operation mode of the line interface. It must be plugged into connector CON3 of the "ST/Up Port Line Interface Sub-Assy with Coding Plug".

Coding plug for
Up interface (NT mode, powered)




| | Up interface (NT mode, powered): |
|---|---|
| TX / RX signals: | TX_A - RX_B - RJ_4: #5 - #1 - #6<br>TX_B - RX_A - RJ_5: #7 - #3 - #8 |
| Power feeding: | U+: #13-#19<br>U-: #14-#20 |
| Line termination: | TX_T, RX_T (#9, #10) unconnected |
| Key signals: | GPI_0 = 0 / GPI_1 = 0<br>K0 - P+ / K1 - P+<br>#17 - #18 - #19 |

CON4 pins 15 and 16 are not connected for 1.5 kV galvanic isolation.

The host processor can detect the used coding plug via GPI_0, GPI_1 signals (derived from key signals K0, K1).

| | | | |
|---|---|---|---|
| Project | XHFC Series Evaluation Kit | | |
| Title | Coding Plug No. 3 for Up interface in NT mode (Rev. 1) | | |
| Size A4 | (c) 2006 Cologne Chip AG | Rev 1.0 | Cologne Chip |
| Date | Friday, January 26, 2007 | Sheet 1 of 1 | |

**Figure 4:** *Coding plug No. 3*

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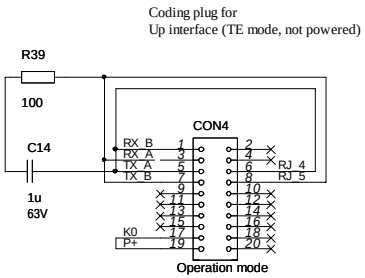
CON4 is used as a coding plug to select a certain operation mode of the line interface. It must be plugged into connector CON3 of the "ST/Up Port Line Interface Sub-Assy with Coding Plug".




| | Up interface (TE mode, not powered): |
|---|---|
| TX / RX signals: | same as shown for powered Up interface |
| Power feeding: | U+, U- (#13, #14) unconnected (no power feeding) |
| Line termination: | TX_T, RX_T (#9, #10) unconnected |
| Key signals: | GPI_0 = 0 / GPI_1 = 1<br>K0 - P+: #17 - #19<br>K1 (#18) unconnected |

CON4 pins 15 and 16 are not connected for 1.5 kV galvanic isolation.

The host processor can detect the used coding plug via GPI_0, GPI_1 signals (derived from key signals K0, K1).

| | | | |
|---|---|---|---|
| Project | XHFC Series Evaluation Kit | | |
| Title | Coding Plug No. 4 for Up interface in TE mode (Rev. 1) | | |
| Size A4 | (c) 2006 Cologne Chip AG | Rev 1.0 | Cologne Chip |
| Date | Friday, January 26, 2007 | Sheet 1 of 1 | |

**Figure 5:** *Coding plug No. 4*

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# 4 Circuitry description

The line interface circuitry shown in Figure 1 on page 6 is a combined circuitry for both S/T and $U_p$ interface mode. A dual S/T transformer module with turns ratio 1:2 is used in both interface modes.

Several coding plugs are shown in Figures 2 . . 5.

## 4.1 Line interface circuitry

Figure 1 shows the line interface circuitry of the S/T Port Line Interface Subassembly with Coding Plug. It can be used for either S/T or $U_p$ interface mode. Further, TE or NT can be selected, power feeding can be switched on or off and line termination can also be enabled or disabled. All these feature selections are accomplished by dedicated coding plugs.

The chip-internal selection of either S/T or $U_p$ interface is an outstanding feature of the XHFC Series microchips of Cologne Chip. A common external circuitry which serves S/T signal characteristics as well as $U_p$ signal characteristics in conjunction with an optimized bill of material – especially just one transformer module for the S/T *and* the $U_p$ circuitry – is the new concept shown in this document.

As this circuitry uses only passive components, the signal range is reduced compared with an amplifying receiver circuitry, but good enough for most applications.

Using a transformer with turns ratio 1:2 even for $U_p$ signaling reduces the transmit amplitude below the recommended value. This reduces the signal range as well. For most applications, signal ranges of up to 1 km are sufficient. This is why the reduced signal range does not mean any restriction in practice.

> **Please note !**
>
> In contrast to the board design of the XHFC Series Evaluation Kit, C1 and C2 should be located as near as possible to the XHFC series microchip pins R_A and R_B.
>
> R1 . . R4 should be located near to the XHFC series microchip pins as well.
>
> In this respect, the XHFC Series Evaluation Kit should not be taken as an example for an optimized product development.

## 4.2 Coding plug

Different features are chosen with a coding plug which has to be inserted into connector CON3. Table 2 shows the signal assignment of the coding plug. Some coding plug options are shown in Figures 2 . . 5.

Every configuration can be established with an individual coding plug. This can be manufactured in a way that a wrong polarity or shifted plug-in cannot occur. In this way, a safe installation is fulfilled even with untrained staff.

Pins 15 and 16 of the coding plug are not connected to achieve 1.5 kV galvanic isolation.

For multi-port applications it is useful to utilize coding plugs with 1 mm or 1.27 mm pin pitch. These can be lined up behind the RJ45 plugs.

## 4.3 RJ45 plug connection

Four different configurations of the RJ45 plug are shown in Figures 2 . . 5. TE mode and NT mode require different wiring for the S/T line interface mode while $U_p$ interface mode shares the same wiring for these two modes. Power feeding connections are different for TE and NT configurations for both S/T and $U_p$ interface modes.

**Table 2:** *Coding plug specification*

| Pin | Signal | Meaning |
|---|---|---|
| #1 | RX_B | Receive signal B of the line interface circuitry |
| #2 | RJ_6 | Signal to RJ45 connector pin 6 |
| #3 | RX_A | Receive signal A of the line interface circuitry |
| #4 | RJ_3 | Signal to RJ45 connector pin 3 |
| #5 | TX_A | Transmit signal A of the line interface circuitry |
| #6 | RJ_4 | Signal to RJ45 connector pin 4 |
| #7 | TX_B | Transmit signal B of the line interface circuitry |
| #8 | RJ_5 | Signal to RJ45 connector pin 5 |
| #9 | TX_T | Line termination to TX_B |
| #10 | RX_T | Line termination to RX_B |
| #11 | S+ | Power feeding for S/T interface mode, positive |
| #12 | S- | Power feeding for S/T interface mode, negative |
| #13 | U+ | Power feeding for $U_p$ interface mode, positive |
| #14 | U- | Power feeding for $U_p$ interface mode, negative |
| #15 | n.c. | Not connected for 1.5 kV galvanic isolation |
| #16 | n.c. | Not connected for 1.5 kV galvanic isolation |
| #17 | K0 | Key contact 0 |
| #18 | K1 | Key contact 1 |
| #19 | P+ | Power feeding source, positive |
| #20 | P- | Power feeding source, negative |

**Table 3:** *RJ45 plug connection*

| RJ45 pin | S/T interface TE mode | S/T interface NT mode | $U_p$ interface |
|---|---|---|---|
| #6 | TX_A | RX_A | – |
| #3 | TX_B | RX_B | – |
| #5 | RX_A | TX_A | TX_B, RX_A |
| #4 | RX_B | TX_B | TX_A, RX_B |

## 4.4 Power feeding

The supply input from CON2 pins 7 and 2 is routed to coding plug pins 19 and 20. For powered line interface modules, either the connection pairs P+ ↔ S+ / P- ↔ S- or P+ ↔ U+ / P- ↔ U- are set up.

As the maximum valid voltage for S/T power feeding is 42 V and the specified $U_p$ voltage is 48 V ± 9 V, a voltage range 39 V . . 42 V is valid for both line interface modes.

Alternatively, an additional Zener diode can be used to achieve a lower voltage for S/T interface selection if the power feeding voltage is increased to 48 V.

## 4.5 Line termination

Line termination can be enabled by the dual switch SW1 on the line interface board for S/T interface in NT mode. The shown coding plug for S/T interface in TE mode disables the switches so that a TE module cannot have line termination by mistake.

Alternatively, the dual switch can be omitted when different coding plugs with and without line termination wiring are provided for S/T line interface in NT mode.

The $U_p$ line interface must always be terminated. A powered $U_p$ interface sets up line termination with the resistors R25 . . R28. For this reason, the dual switch SW1 is disabled with the coding plug. The unpowered $U_p$ interface is terminated via resistor R36 which is populated on the coding plug.

## 4.6 Key contacts

Two key contacts are available at the coding plug to report the chosen interface configuration to the host processor. The key signals K0 and K1 and their derived signals GPI_0 and GPI_1 are shown in table 4.

**Table 4:** *Key signals*

| K0 | K1 | GPI_0 | GPI_1 | Meaning |
|---|---|---|---|---|
| open | open | '1' | '1' | S/T interface, TE mode |
| open | P+ | '1' | '0' | S/T interface, NT mode |
| P+ | P+ | '0' | '0' | $U_p$ interface, powered, NT mode |
| P+ | open | '0' | '1' | $U_p$ interface, not powered, TE mode |

Three circuitry variants are shown in Figure 1 to convert the key signals K0 and K1 to GPI_0 and GPI_1.

Variation A implements a DC isolation between line side and chip side of the circuitry. Two optical couplers are used to transfer the key signals.

Variation B is a simple DC coupled circuitry which interconnects the power source P- with ground. As all variants are implemented on the evaluation board, resistors R33 . . R35 are THT type for 1.5 kV galvanic isolation.

Variation C is another simple DC coupled circuitry which interconnects the power source P+ with ground. As all variants are implemented on the evaluation board, resistors R36 . . R38 are THT type

for 1.5 kV galvanic isolation.

> **Please note !**
>
> Variations B and C interconnect ground of the host system with either P- or P+. This is only allowed when not both ground and one pole of the power source are earth-connected.
>
> If P- is earth-connected, Variation C must not be chosen! Otherwise P+ and P- are short-circuited via R38.
>
> If P+ is earth-connected, Variation B must not be chosen! Otherwise P+ and P- are short-circuited via R35.

Two LEDs are used to indicate the current key signals. They are connected to the GPI_0 and GPI_1 signals of connector CON1. Alternatively, they can be placed beside or inside the RJ45 plug package. [2] Then, it would be useful to wire them directly to the K0 and K1 signals.

[2] 1.5 kV overvoltage protection between LEDs and RJ45-Signals must be ensured.

# 5 Module layout

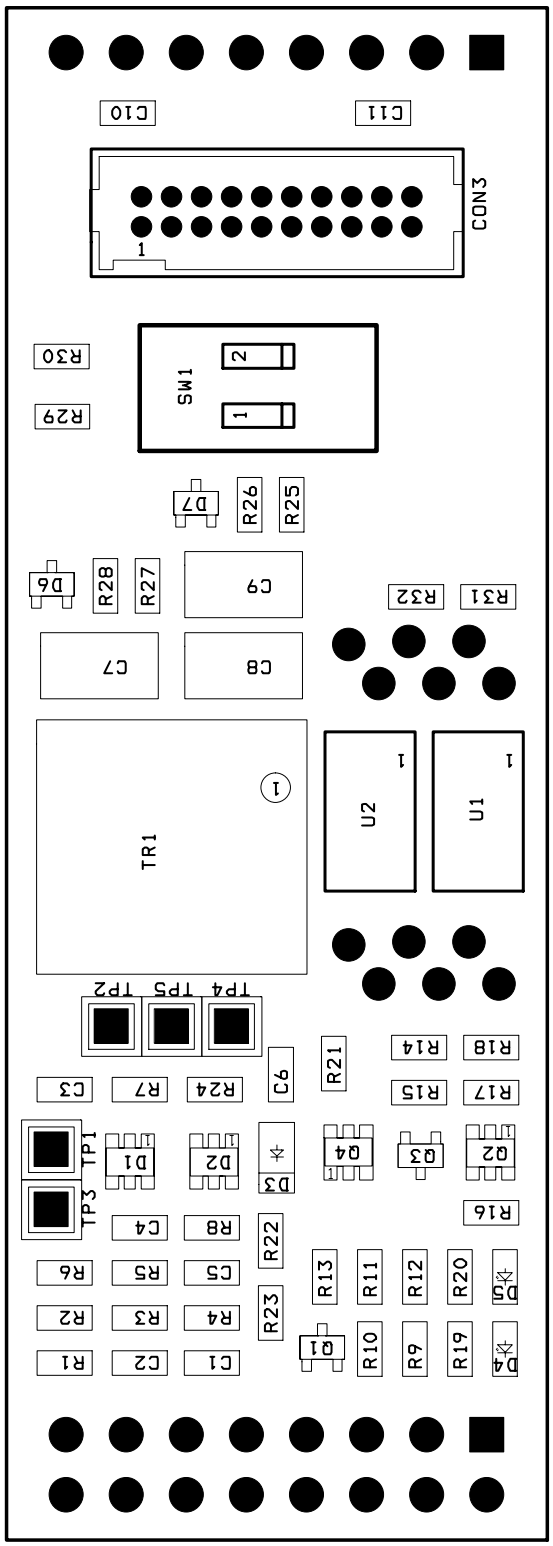


**Figure 6:** *S/T Port Line Interface Subassembly with Coding Plug board (top side components)*

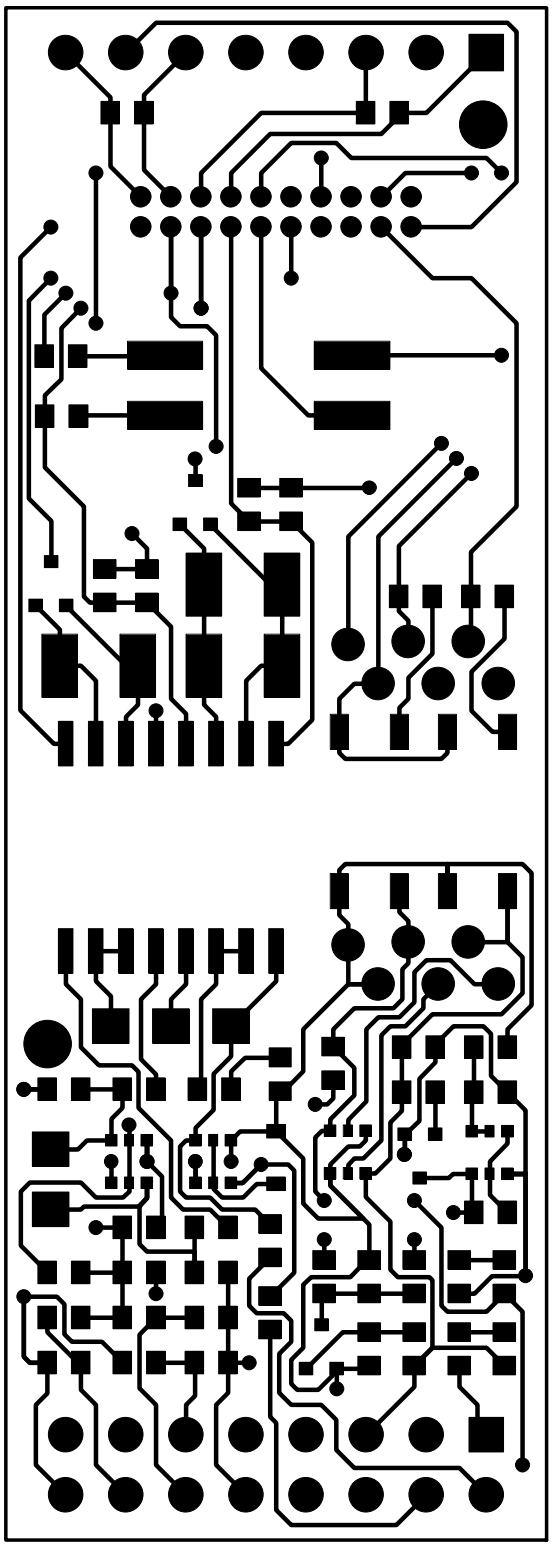

**Figure 7:** *S/T Port Line Interface Subassembly with Coding Plug board (top side traces)*

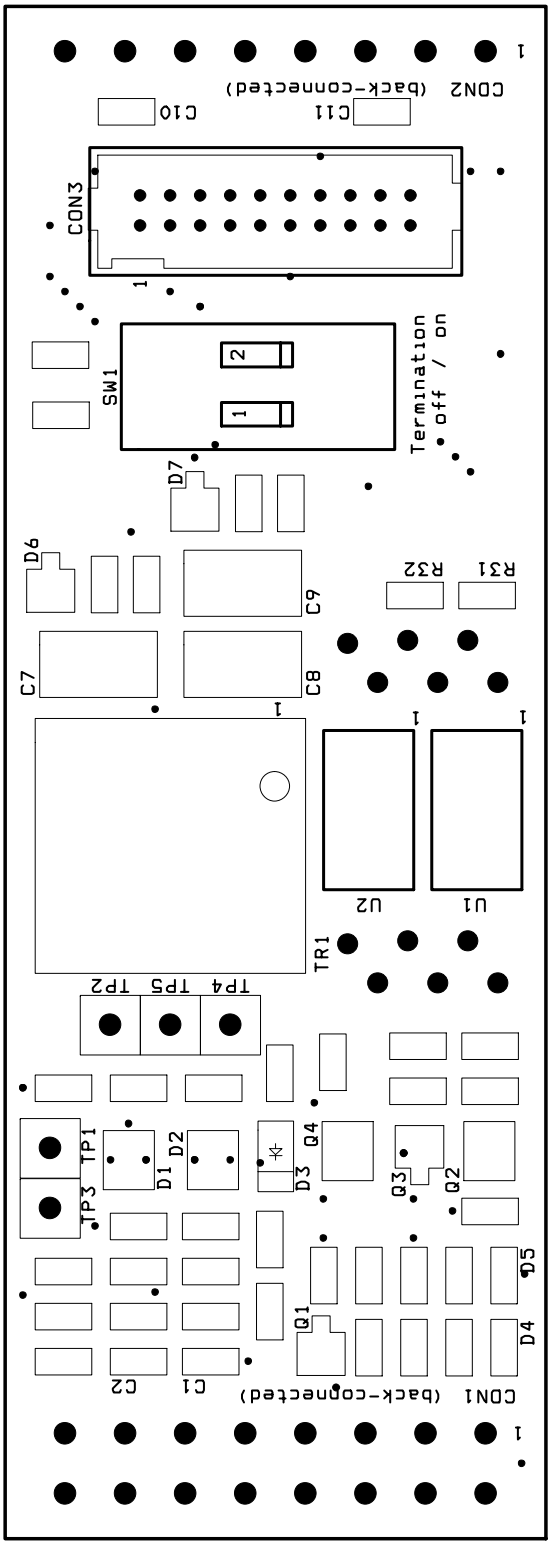


**Figure 8:** *S/T Port Line Interface Subassembly with Coding Plug board (top side inscription)*

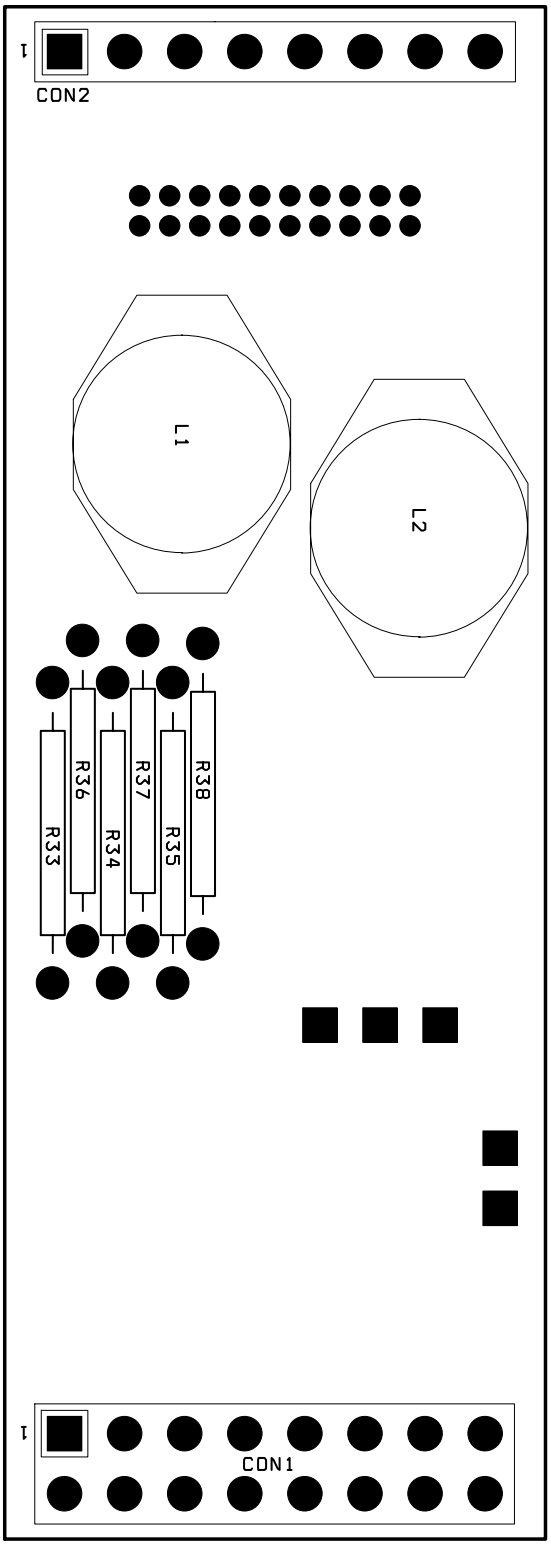


**Figure 9:** *S/T Port Line Interface Subassembly with Coding Plug board (bottom side components)*

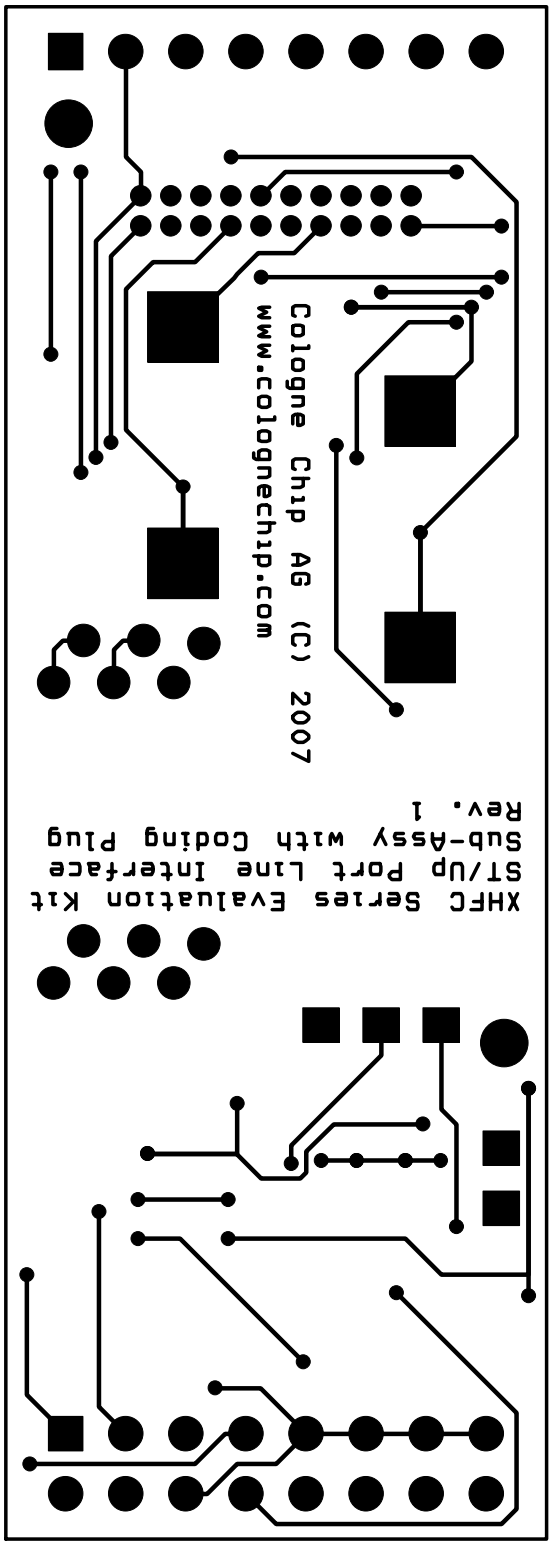


**Figure 10:** *S/T Port Line Interface Subassembly with Coding Plug board (bottom side traces)*

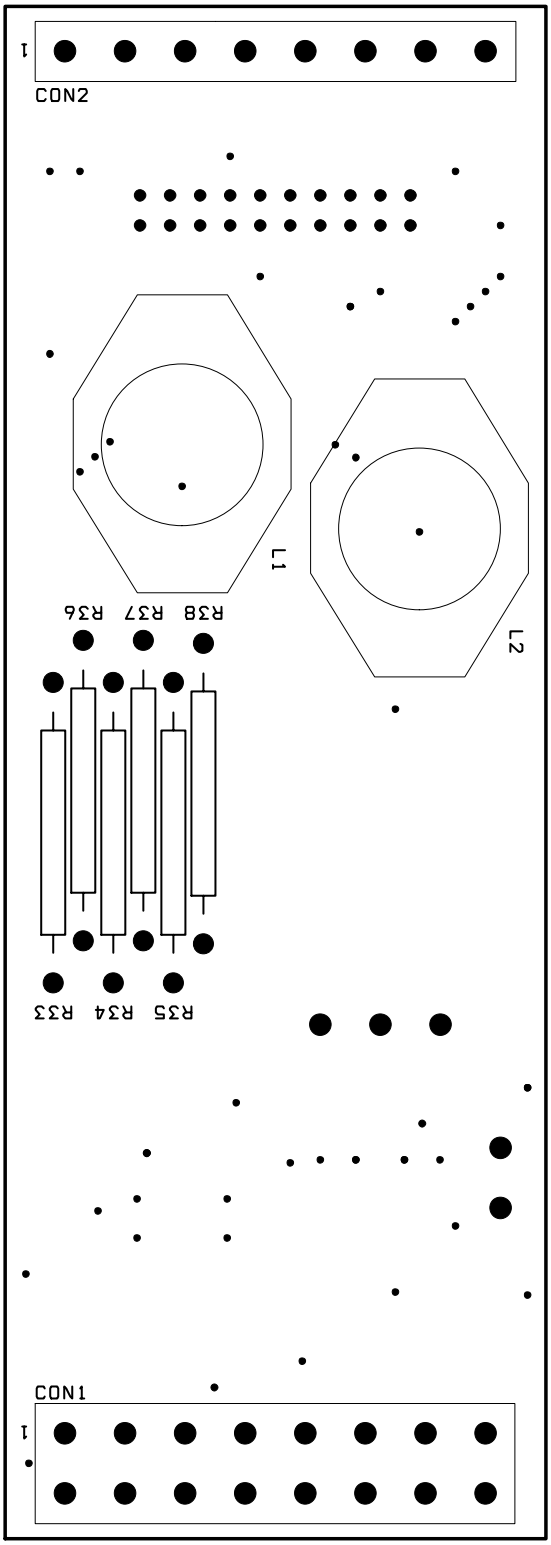


**Figure 11:** *S/T Port Line Interface Subassembly with Coding Plug board (bottom side inscription)*

# 6 Coding plug layouts

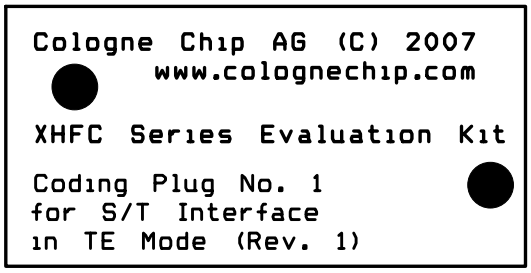


**Figure 12:** *Coding Plug No. 1 for S/T interface in TE mode (top side inscription)*

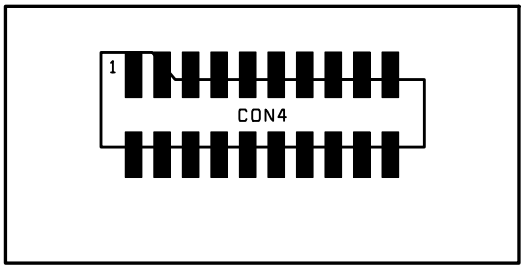


**Figure 13:** *Coding Plug No. 1 for S/T interface in TE mode (bottom side components)*

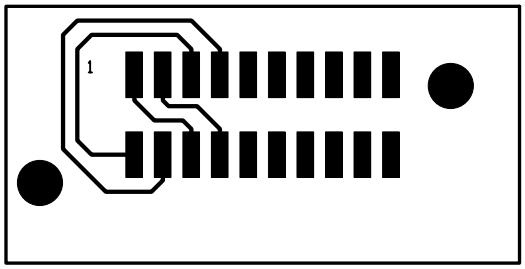


**Figure 14:** *Coding Plug No. 1 for S/T interface in TE mode (bottom side components)*

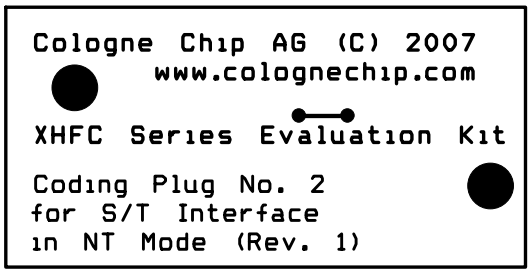


**Figure 15:** *Coding Plug No. 2 for S/T interface in NT mode (top side inscription)*

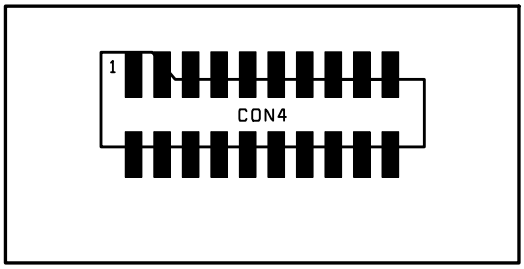


**Figure 16:** *Coding Plug No. 2 for S/T interface in NT mode (bottom side components)*

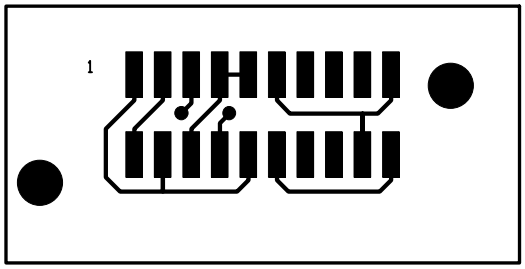


**Figure 17:** *Coding Plug No. 2 for S/T interface in NT mode (bottom side components)*

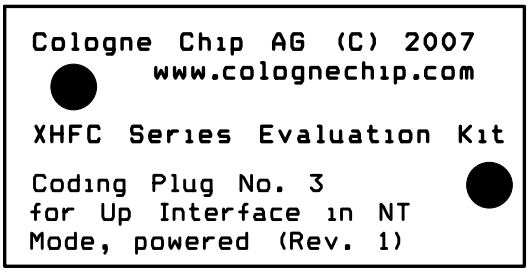


**Figure 18:** *Coding Plug No. 3 for $U_p$ interface in NT mode (top side inscription)*

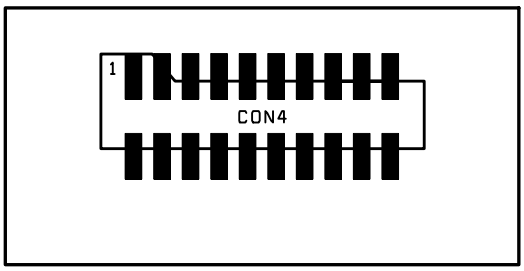


**Figure 19:** *Coding Plug No. 3 for $U_p$ interface in NT mode (bottom side components)*

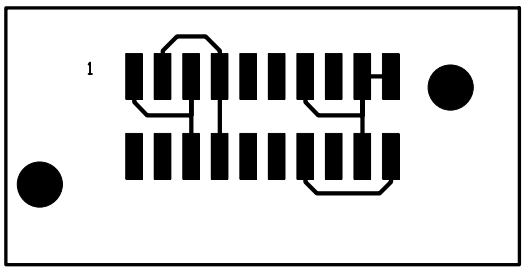


**Figure 20:** *Coding Plug No. 3 for $U_p$ interface in NT mode (bottom side components)*

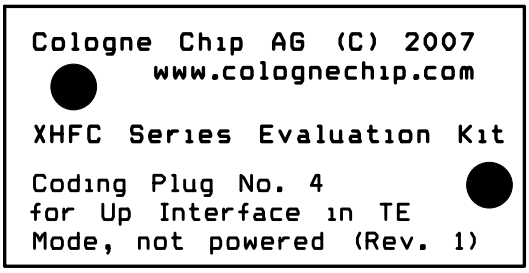


**Figure 21:** *Coding Plug No. 4 for $U_p$ interface in TE mode (top side inscription)*

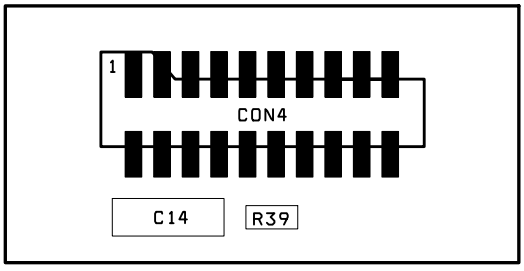


**Figure 22:** *Coding Plug No. 4 for $U_p$ interface in TE mode (bottom side components)*

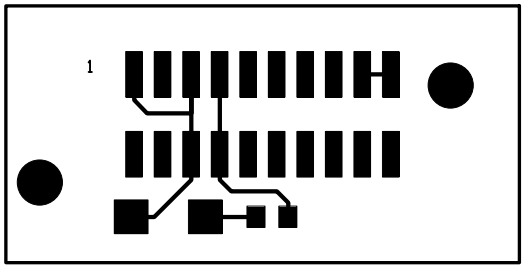


**Figure 23:** *Coding Plug No. 4 for $U_p$ interface in TE mode (bottom side components)*

## References

[1] Cologne Chip AG. *XHFC Series Evaluation Kit. XHFC-1SU Evaluation Board Rev. 1*, June 2006.

[2] Cologne Chip AG. *XHFC Series Evaluation Kit. XHFC-2SU Evaluation Board Rev. 1*, June 2006.

[3] Cologne Chip AG. *XHFC Series Evaluation Kit. XHFC-4SU Evaluation Board Rev. 1*, June 2006.


**Cologne Chip AG**

**Line Interface Subassembly**