Cologne Chip

Layer - 1 Conformance Test

for the S/T interface of
XHFC - 1SU / XHFC - 2SU / XHFC - 2S4U / XHFC - 4SU
ISDN Basic Rate Controllers

measured with
S/T Port Line Interface Subassembly Revision 2
of the XHFC Evaluation Kit

Test Report ✦ August 2006

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1 Overview

This document contains the test report and the measurement results for the S/T line interface of the single-port Basic Rate Controller IC XHFC-1SU [1] and the multi-port Basic Rate Controller ICs XHFC-2SU [3], XHFC-2S4U and XHFC-4SU [2] of Cologne Chip.

All measurements were executed with the XHFC-4SU Evaluation Board Revision 1 [5] with S/T Port Line Interface Subassembly Revision 2 [4] (please refer to schematic in appendix A on page 57). Both PCBs are part of the XHFC Series Evaluation Kit. The line interfaces of all XHFC series microchips are identical.

The device under test has successfully passed all layer 1 conformance tests according to the CTR 3 / TBR 3 [6] specification. The ISDN controller microchips of the XHFC series are compliant to the hardware specifications of the ISDN standards I.430 [7].

The ISDN S/T conformance test has been made at the test laboratory for telecom interfaces of the TÜV Rheinland Product Safety in Cologne, Germany in August 2006. The TÜV labs are a certified body for Telecom Approvals. All tests were made using a Tektronix K 1403 conformance tester. The test results and measurement results shown in this document were saved from the test equipment on August 23h, 2006.

Test Laboratory

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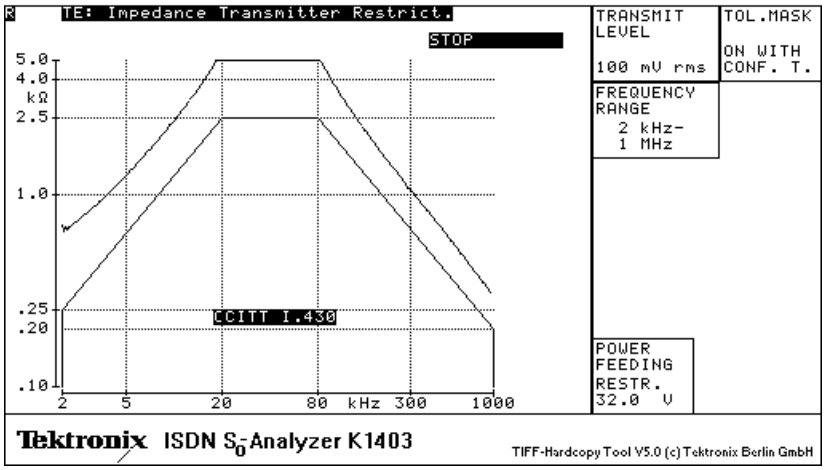
2 Output impedance

V30-12.4

Test A: Output impedance when transmitting a binary one in state F3, restricted power at 32 V.

Conformance PASSED



Measurement finished. Expected TAV-count reached.

30-12.8

Test B: Output impedance when transmitting a binary zero, positive pulses into a 50 Ω load, restricted power at 32 V.

Double pulses into 50 Ω (R+,R-,R+-), isolated pulses (R+) w. loop.

Conformance PASSED

R(+/-) = 0.000000 Ω	R(+) = 0.000000 Ω	R(-) = 37.969784 Ω

Measurement finished. Expected TAV-count reached.

V30-12.12

Test B: Output impedance when transmitting a binary zero, negative pulses into a 50 Ω load, restricted power at 32 V.

Double pulses into 50 Ω (R+,R-,R+-), isolated pulses (R-) w. loop.

Conformance PASSED

R(+/-) = 0.000000 Ω	R(+) = 37.852459 Ω	R(-) = 0.000000 Ω

Measurement finished. Expected TAV-count reached.

V30-12.16

Test B: Output impedance when transmitting a binary zero, positive pulses into a 400 Ω load, restricted power at 32 V.

Double pulses into 400 Ω (R+,R-,R+-), isolated pulses (R+) w. loop.

Conformance PASSED

R(+/-) = 0.000000 Ω	R(+) = 0.000000 Ω	R(-) = 39.043797 Ω

Measurement finished. Expected TAV-count reached.

V30-12.20

Test B: Output impedance when transmitting a binary zero, negative pulses into a 400 Ω load, restricted power at 32 V.

Double pulses into 400 Ω (R+,R-,R+-), isolated pulses (R-) w. loop.

Conformance PASSED

R(+/-) = 0.000000 Ω	R(+) = 38.720039 Ω	R(-) = 0.000000 Ω

Measurement finished. Expected TAV-count reached.

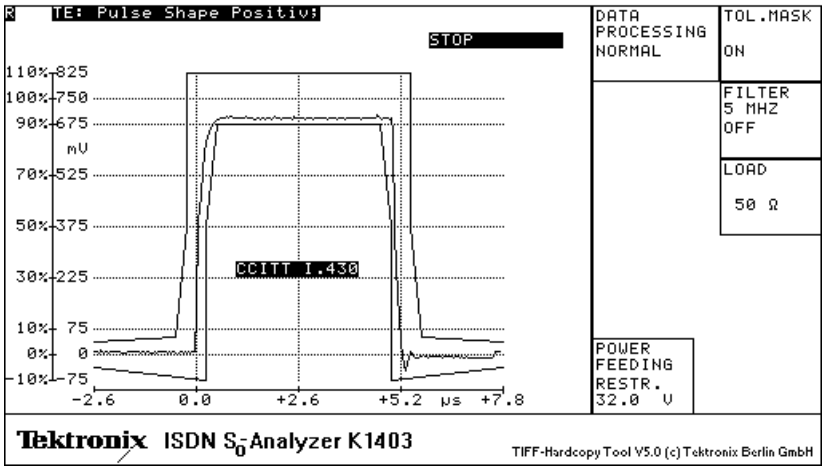
3 Pulse shape

V30-13.4

Pulse shape and amplitude for positive pulses, restricted power at 32 V.

Multi Periodic Sampling (MPS), 12 Bit/24 MHz and 1st double pulse, 12 Bit/16 MHz (#).

Conformance PASSED



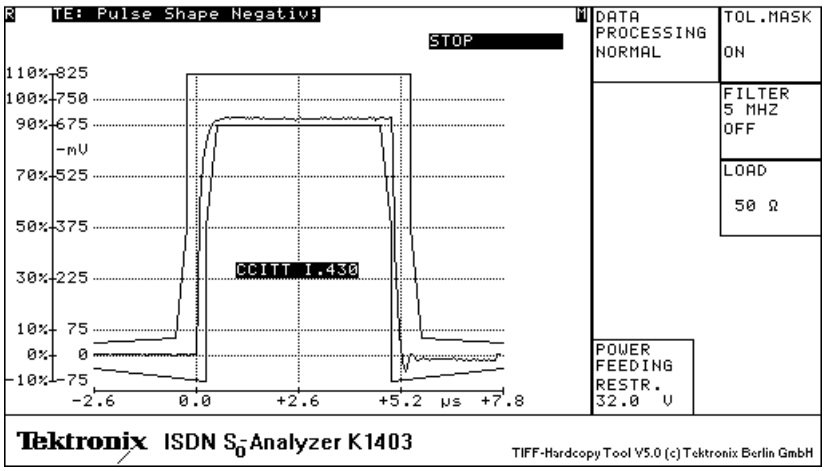
Measurement finished. Expected TAV-count reached.

V30-13.8

Pulse shape and amplitude for negative pulses, restricted power at 32 V.

Multi Periodic Sampling (MPS), 12 Bit/24 MHz and 1st double pulse, 12 Bit / 16 MHz (#).

Conformance PASSED



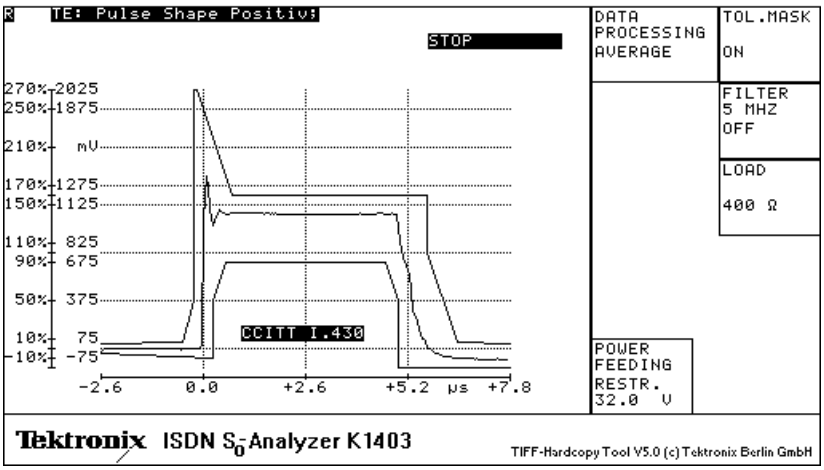
Measurement finished. Expected TAV-count reached.

V30-13.12

Test A: Voltage on a 400 Ω load (pulse shape) for positive pulses, restricted power at 32 V.

Multi Periodic Sampling (MPS), 12 Bit/24 MHz.

Conformance PASSED



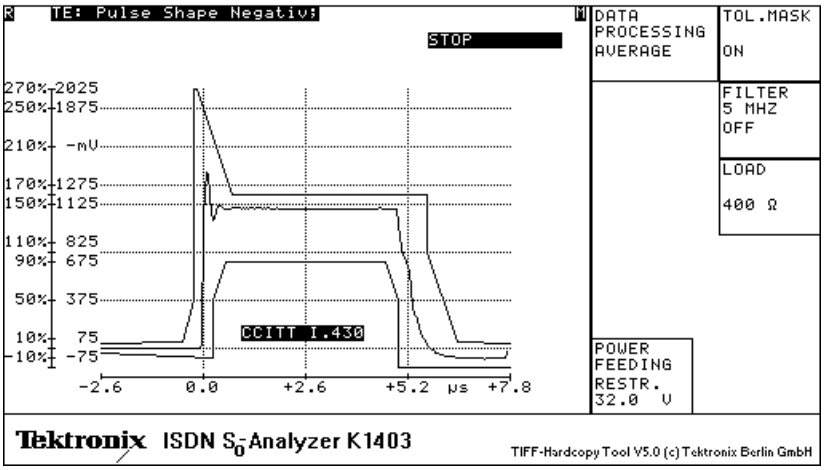
Measurement finished. Expected TAV-count reached.

V30-13.16

Test A: Voltage on a 400 Ω load (pulse shape) for negative pulses, restricted power at 32 V.

Multi Periodic Sampling (MPS), 12 Bit/24 MHz.

Conformance PASSED



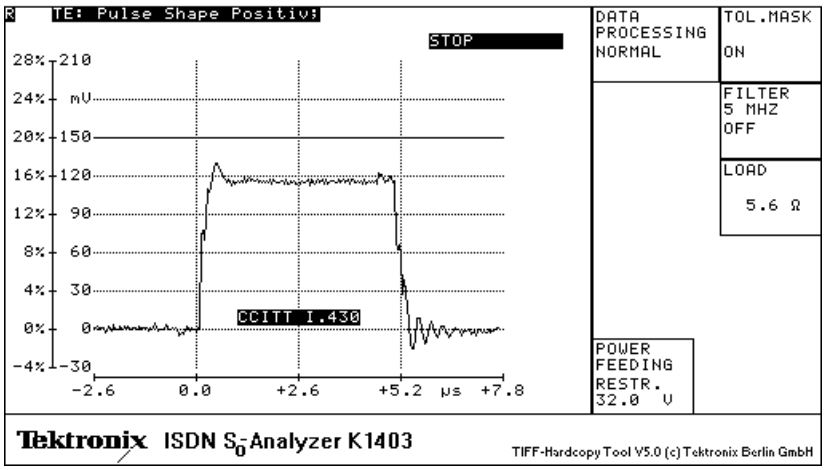
Measurement finished. Expected TAV-count reached.

V30-13.20

Test B: Voltage on a 5.6 Ω load (pulse shape) for positive pulses, restricted power at 32 V.

Multi Periodic Sampling (MPS), 12 Bit/24 MHz.

Conformance PASSED



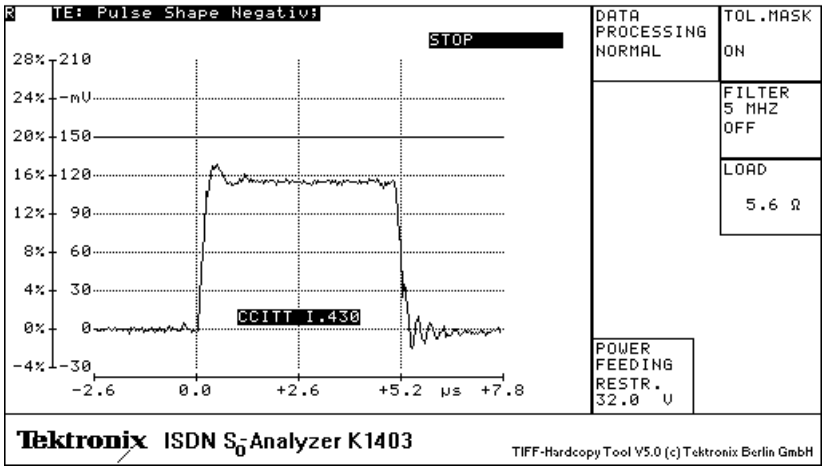
Measurement finished. Expected TAV-count reached.

V30-13.24

Test B: Voltage on a 5.6 Ω load (pulse shape) for negative pulses, restricted power at 32 V.

Multi Periodic Sampling (MPS), 12 Bit/24 MHz.

Conformance PASSED



Measurement finished. Expected TAV-count reached.

4 Pulse amplitude

V30-14.1

Pulse amplitude, normal power at 42 V.

Multi Periodic Sampling (MPS), 12 Bit/16 MHz.

Conformance PASSED

$\Delta U_+/U_{nom} = -7.607476\%$	$\Delta U_-/U_{nom} = -8.184329\%$

Measurement finished. Expected TAV-count reached.

V30-14.2

Pulse amplitude, normal power at 24 V

Multi Periodic Sampling (MPS), 12 Bit / 16 MHz.

Conformance PASSED

$\Delta U_+/U_{nom} = -7.669433\%$	$\Delta U_-/U_{nom} = -8.250562\%$

Measurement finished. Expected TAV-count reached.

V30-14.4

Pulse amplitude, restricted power at 32 V

Multi Periodic Sampling (MPS), 12 Bit / 16 MHz.

Conformance PASSED

$\Delta dU_+/U_{nom} = -7.684175\%$	$\Delta U_-/U_{nom} = -8.171725\%$

Measurement finished. Expected TAV-count reached.

5 Pulse unbalance of an isolated couple of pulses

V30-14.5

Pulse unbalance of an isolated couple of pulses, normal power at 42 V.

Multi Periodic Sampling (MPS), 12 Bit/16 MHz, digital integration of 1st or 2nd double pulse of INFO.

Conformance PASSED

$$\Delta f / F_{nom} = -2.311680\%$$

Measurement finished. Expected TAV-count reached.

V30-14.6

Pulse unbalance of an isolated couple of pulses, normal power at 24 V.

Multi Periodic Sampling (MPS), 12 Bit/16 MHz, digital integration of 1st or 2nd double pulse of INFO.

Conformance PASSED

$$\Delta f / F_{nom} = -3.158667\%$$

Measurement finished. Expected TAV-count reached.

V30-14.8

Pulse unbalance of an isolated couple of pulses, restricted power at 32 V.

Multi Periodic Sampling (MPS), 12 Bit/16 MHz, digital integration of 1st or 2nd double pulse of INFO.

Conformance PASSED

$$\Delta f / F_{nom} = -2.386763\%$$

Measurement finished. Expected TAV-count reached.

6 Transmitter output longitudinal conversion loss

V30-15.1

Transmitter output longitudinal conversion loss in state F3, normal power at 42 V.

Conformance PASSED

Measurement finished. Expected TAV-count reached.

V30-15.2

Transmitter output longitudinal conversion loss in state F3, normal power at 24 V.

Conformance PASSED

Measurement finished. Expected TAV-count reached.

V30-15.3

Transmitter output longitudinal conversion loss in state F3, restricted power at 42 V.

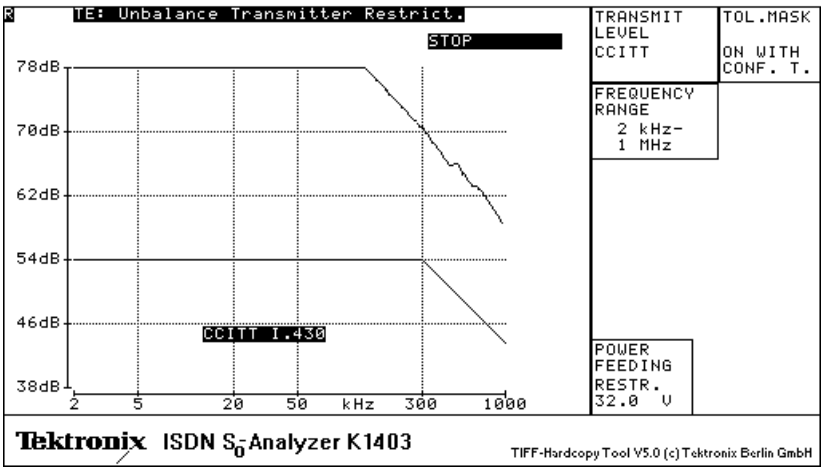
Conformance PASSED

Measurement finished. Expected TAV-count reached.

V30-15.4

Transmitter output longitudinal conversion loss in state F3, restricted power at 32 V.

Conformance PASSED



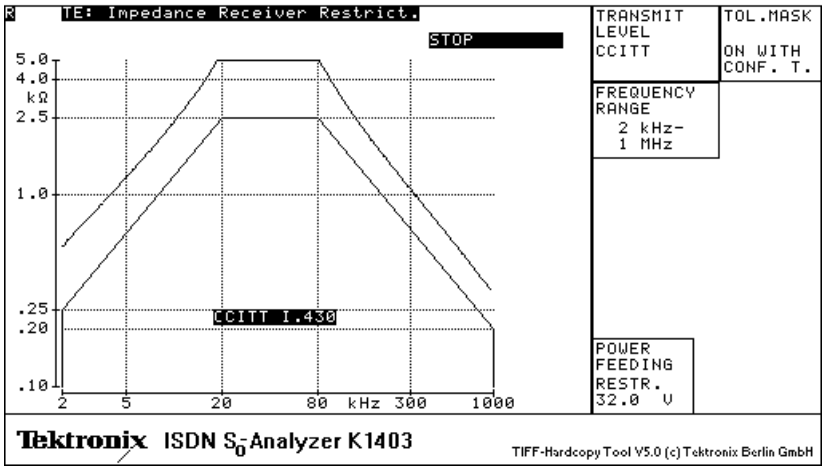
Measurement finished. Expected TAV-count reached.

7 Receiver input impedance

V30-16.4

Test A: Receiver input impedance in state F3, restricted power at 32 V.

Conformance PASSED



Measurement finished. Expected TAV-count reached.

8 Receiver longitudinal conversion loss

V30-18.1U

Receiver unbalance about earth (longitudinal conversion loss) in state F3, normal power at 42 V.

Conformance PASSED

Measurement finished. Expected TAV-count reached.

V30-18.2U

Receiver unbalance about earth (longitudinal conversion loss) in state F3, normal power at 24 V.

Conformance PASSED

Measurement finished. Expected TAV-count reached.

V30-18.3U

Receiver unbalance about earth (longitudinal conversion loss) in state F3, restricted power at 42 V.

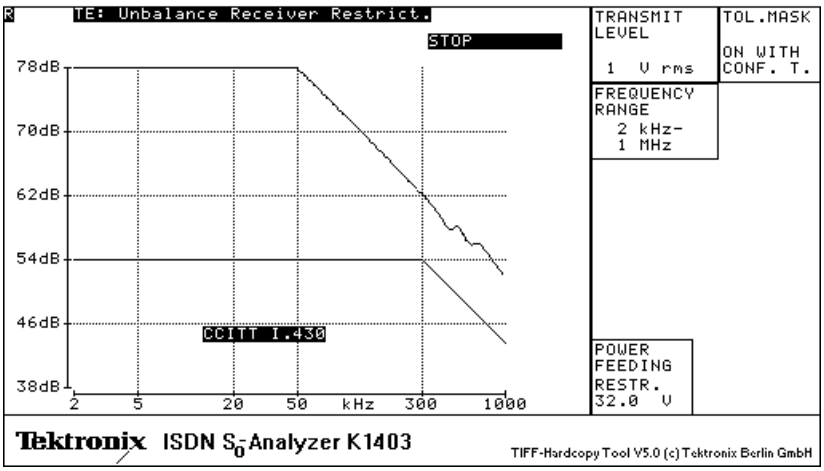
Conformance PASSED

Measurement finished. Expected TAV-count reached.

V30-18.4U

Receiver unbalance about earth (longitudinal conversion loss) in state F3, restricted power at 32 V.

Conformance PASSED



Measurement finished. Expected TAV-count reached.

9 Input to output offset

9.1 Config. I: Binary ones, different jitter

V30-11.4a

Input to output offset, point to point configuration (high cap. cable with 6 dB attenuation) with an input sequence of continuous frames with all binary ones in D-, D-Echo and both B-channels, restricted power at 32 V.

config. I, jitter 5 Hz / 0,5 UI

Conformance PASSED

$t_{min} = -2.146405\%$	$t_{max} = 1.453641\%$	$t_{ava} = 1.053616\%$

Measurement finished. Expected TAV-count reached.

V30-11.4b

Input to output offset, point to point configuration (high cap. cable with 6 dB attenuation) with an input sequence of continuous frames with all binary ones in D-, D-Echo and both B-channels, restricted power at 32 V.

config. I, jitter 20 Hz / 0,125 UI

Conformance PASSED

$t_{min} = -2.546384\%$	$t_{max} = 1.453641\%$	$t_{ava} = 0.653592\%$

Measurement finished. Expected TAV-count reached.

V30-11.4c

Input to output offset, point to point configuration (high cap. cable with 6 dB attenuation) with an input sequence of continuous frames with all binary ones in D-, D-Echo and both B-channels, restricted power at 32 V.

config. I, jitter 50 Hz / 0,05 UI

Conformance PASSED

$t_{min} = -2.346371\%$	$t_{max} = 1.653653\%$	$t_{ava} = -1.146381\%$

Measurement finished. Expected TAV-count reached.

V30-11.4d

Input to output offset, point to point configuration (high cap. cable with 6 dB attenuation) with an input sequence of continuous frames with all binary ones in D-, D-Echo and both B-channels, restricted power at 32 V.

config. I, jitter 2015 Hz / 0,05 UI

Conformance PASSED

$t_{min} = -3.546368\%$	$t_{max} = 2.053616\%$	$t_{ava} = -0.746371\%$

Measurement finished. Expected TAV-count reached.

9.2 Config. I: Octet 0x0AA, different jitter

V30-11.24a

Input to output offset, point to point configuration (high cap. cable with 6 dB attenuation) with an input sequence of continuous frames with the octet 0x0AA in both B-channels and binary ones in the D-and D-Echo channels, restricted power at 32 V.

config. I, jitter 5 Hz / 0,5 UI

Conformance PASSED

$t_{min} = -1.946393\%$	$t_{max} = 1.653653\%$	$t_{ava} = -0.746371\%$

Measurement finished. Expected TAV-count reached.

V30-11.24b

Input to output offset, point to point configuration (high cap. cable with 6 dB attenuation) with an input sequence of continuous frames with the octet 0x0AA in both B-channels and binary ones in the D-and D-Echo channels, restricted power at 32 V.

config. I, jitter 20 Hz / 0,125 UI

Conformance PASSED

$t_{min} = -5.546376\%$	$t_{max} = 1.653653\%$	$t_{ava} = -0.346393\%$

Measurement finished. Expected TAV-count reached.

V30-11.24c

Input to output offset, point to point configuration (high cap. cable with 6 dB attenuation) with an input sequence of continuous frames with the octet 0x0AA in both B-channels and binary ones in the D-and D-Echo channels, restricted power at 32 V.

config. I, jitter 50 Hz / 0,05 UI

Conformance PASSED

$t_{min} = -1.946393\%$	$t_{max} = 1.653653\%$	$t_{ava} = -1.146381\%$

Measurement finished. Expected TAV-count reached.

V30-11.24d

Input to output offset, point to point configuration (high cap. cable with 6 dB attenuation) with an input sequence of continuous frames with the octet 0x0AA in both B-channels and binary ones in the D-and D-Echo channels, restricted power at 32 V.

config. I, jitter 2015 Hz / 0,05 UI

Conformance PASSED

$t_{min} = -5.746388\%$	$t_{max} = 3.453641\%$	$t_{ava} = -0.546405\%$

Measurement finished. Expected TAV-count reached.

9.3 Config. I: Binary zeros, different jitter

V30-11.44a

Input to output offset, point to point configuration (high cap. cable with 6 dB attenuation) with an input sequence of continuous frames with all binary zeroes in D-, D-Echo and both B-channels, restricted power at 32 V.

config. I, jitter 5 Hz / 0,5 UI

Conformance PASSED

$t_{min} = -1.546384\%$	$t_{max} = 2.053616\%$	$t_{ava} = -1.146381\%$

Measurement finished. Expected TAV-count reached.

V30-11.44b

Input to output offset, point to point configuration (high cap. cable with 6 dB attenuation) with an input sequence of continuous frames with all binary zeroes in D-, D-Echo and both B-channels, restricted power at 32 V.

config. I, jitter 20 Hz / 0,125 UI

Conformance PASSED

$t_{min} = -1.946393\%$	$t_{max} = 2.053616\%$	$t_{ava} = 0.053616\%$

Measurement finished. Expected TAV-count reached.

V30-11.44c

Input to output offset, point to point configuration (high cap. cable with 6 dB attenuation) with an input sequence of continuous frames with all binary zeroes in D-, D-Echo and both B-channels, restricted power at 32 V.

config. I, jitter 50 Hz / 0,05 UI

Conformance PASSED

$t_{min} = -2.546384\%$	$t_{max} = 1.853604\%$	$t_{ava} = 0.653592\%$

Measurement finished. Expected TAV-count reached.

V30-11.44d

Input to output offset, point to point configuration (high cap. cable with 6 dB attenuation) with an input sequence of continuous frames with all binary zeroes in D-, D-Echo and both B-channels, restricted power at 32 V.

config. I, jitter 2015 Hz / 0,05 UI

Conformance PASSED

$t_{min} = -5.746388\%$	$t_{max} = 1.853604\%$	$t_{ava} = 0.653592\%$

Measurement finished. Expected TAV-count reached.

9.4 Config. I: $2^{19} - 1$ PRBS, different jitter

V30-11.64a

Input to output offset, point to point configuration (high cap. cable with 6 dB attenuation) with an input sequence of continuous frames with a $2^{19} - 1$ PRBS in D-, D-Echo and both B-channels, restricted power at 32 V.

config. I, jitter 5 Hz / 0,5 UI

Conformance PASSED

$t_{min} = -2.346371\%$	$t_{max} = 2.853604\%$	$t_{ava} = 0.053616\%$

Measurement finished. Expected TAV-count reached.

V30-11.64b

Input to output offset, point to point configuration (high cap. cable with 6 dB attenuation) with an input sequence of continuous frames with a $2^{19} - 1$ PRBS in D-, D-Echo and both B-channels, restricted power at 32 V.

config. I, jitter 20 Hz / 0,125 UI

Conformance PASSED

$t_{min} = -2.546384\%$	$t_{max} = 2.653592\%$	$t_{ava} = -0.546405\%$

Measurement finished. Expected TAV-count reached.

V30-11.64c

Input to output offset, point to point configuration (high cap. cable with 6 dB attenuation) with an input sequence of continuous frames with a $2^{19} - 1$ PRBS in D-, D-Echo and both B-channels, restricted power at 32 V.

config. I, jitter 50 Hz / 0,05 UI

Conformance PASSED

$t_{min} = -2.346371\%$	$t_{max} = 2.853604\%$	$t_{ava} = 0.453641\%$

Measurement finished. Expected TAV-count reached.

V30-11.64d

Input to output offset, point to point configuration (high cap. cable with 6 dB attenuation) with an input sequence of continuous frames with a $2^{19}-1$ PRBS in D-, D-Echo and both B-channels, restricted power at 32 V.

config. I, jitter 2015 Hz / 0,05 UI

Conformance PASSED

$t_{min} = -2.746381\%$	$t_{max} = 2.853604\%$	$t_{ava} = 0.853604\%$

Measurement finished. Expected TAV-count reached.

9.5 Config. II: Binary ones, different jitter

V30-11.8a

Input to output offset, short passive bus configuration (high cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with an input sequence of continuous frames with all binary ones in D-, D-Echo and both B-channels, restricted power at 32 V.

config. II, jitter 5 Hz / 0,5 UI

Conformance PASSED

$t_{min} = 0.588020\%$	$t_{max} = 8.588031\%$	$t_{ava} = 6.588033\%$

Measurement finished. Expected TAV-count reached.

V30-11.8b

Input to output offset, short passive bus configuration (high cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with an input sequence of continuous frames with all binary ones in D-, D-Echo and both B-channels, restricted power at 32 V.

config. II, jitter 20 Hz / 0,125 UI

Conformance PASSED

$t_{min} = -0.411986\%$	$t_{max} = 8.788033\%$	$t_{ava} = 7.988021\%$

Measurement finished. Expected TAV-count reached.

V30-11.8c

Input to output offset, short passive bus configuration (high cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with an input sequence of continuous frames with all binary ones in D-, D-Echo and both B-channels, restricted power at 32 V.

config. II, jitter 50 Hz / 0,05 UI

Conformance PASSED

$t_{min} = 0.788022\%$	$t_{max} = 8.788033\%$	$t_{ava} = 7.188031\%$

Measurement finished. Expected TAV-count reached.

V30-11.8d

Input to output offset, short passive bus configuration (high cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with an input sequence of continuous frames with all binary ones in D-, D-Echo and both B-channels, restricted power at 32 V.

config. II, jitter 2015 Hz / 0,05 UI

Conformance PASSED

$t_{min} = 0.588020\%$	$t_{max} = 8.588031\%$	$t_{ava} = 5.388024\%$

Measurement finished. Expected TAV-count reached.

9.6 Config. II: Octet 0x0AA, different jitter

V30-11.28a

Input to output offset, short passive bus configuration (low cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus, with an input sequence of continuous frames with the octet 0x0AA in both B-channels and binary ones in the D- and D-Echo channels, restricted power at 32 V.

config. II, jitter 5 Hz / 0,5 UI

Conformance PASSED

$t_{min} = 0.788022\%$	$t_{max} = 8.788033\%$	$t_{ava} = 8.388015\%$

Measurement finished. Expected TAV-count reached.

V30-11.28b

Input to output offset, short passive bus configuration (low cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus, with an input sequence of continuous frames with the octet 0x0AA in both B-channels and binary ones in the D- and D-Echo channels, restricted power at 32 V.

config. II, jitter 20 Hz / 0,125 UI

Conformance PASSED

$t_{min} = 0.588020\%$	$t_{max} = 8.588031\%$	$t_{ava} = 5.788020\%$

Measurement finished. Expected TAV-count reached.

V30-11.28c

Input to output offset, short passive bus configuration (low cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus, with an input sequence of continuous frames with the octet 0x0AA in both B-channels and binary ones in the D- and D-Echo channels, restricted power at 32 V.

config. II, jitter 50 Hz / 0,05 UI

Conformance PASSED

$t_{min} = 2.188024\%$	$t_{max} = 8.588031\%$	$t_{ava} = 7.388022\%$

Measurement finished. Expected TAV-count reached.

V30-11.28d

Input to output offset, short passive bus configuration (low cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus, with an input sequence of continuous frames with the octet 0x0AA in both B-channels and binary ones in the D- and D-Echo channels, restricted power at 32 V.

config. II, jitter 2015 Hz / 0,05 UI

Conformance PASSED

$t_{min} = 2.388026\%$	$t_{max} = 8.788033\%$	$t_{ava} = 5.988023\%$

Measurement finished. Expected TAV-count reached.

9.7 Config. II: Binary zeros, different jitter

V30-11.48a

Input to output offset, short passive bus configuration (high cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus, with an input sequence of continuous frames with all binary zeroes in D-, D-Echo and both B-channels, restricted power at 32 V.

config. II, jitter 5 Hz / 0,5 UI

Conformance PASSED

$t_{min} = 0.788022\%$	$t_{max} = 8.788033\%$	$t_{ava} = 5.988023\%$

Measurement finished. Expected TAV-count reached.

V30-11.48b

Input to output offset, short passive bus configuration (high cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus, with an input sequence of continuous frames with all binary zeroes in D-, D-Echo and both B-channels, restricted power at 32 V.

config. II, jitter 20 Hz / 0,125 UI

Conformance PASSED

$t_{min} = 0.588020\%$	$t_{max} = 8.588031\%$	$t_{ava} = 6.188014\%$

Measurement finished. Expected TAV-count reached.

V30-11.48c

Input to output offset, short passive bus configuration (high cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus, with an input sequence of continuous frames with all binary zeroes in D-, D-Echo and both B-channels, restricted power at 32 V.

config. II, jitter 50 Hz / 0,05 UI

Conformance PASSED

$t_{min} = 0.788022\%$	$t_{max} = 8.788033\%$	$t_{ava} = 7.988021\%$

Measurement finished. Expected TAV-count reached.

V30-11.48d

Input to output offset, short passive bus configuration (high cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus, with an input sequence of continuous frames with all binary zeroes in D-, D-Echo and both B-channels, restricted power at 32 V.

config. II, jitter 2015 Hz / 0,05 UI

Conformance PASSED

$t_{min} = -0.611989\%$	$t_{max} = 8.588031\%$	$t_{ava} = 6.188014\%$

Measurement finished. Expected TAV-count reached.

9.8 Config. II: $2^{19} - 1$ PRBS, different jitter

V30-11.68a

Input to output offset, short passive bus configuration (high cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with an input sequence of continuous frames with a $2^{19} - 1$ PRBS in D-, D-Echo and both B-channels, restricted power at 32 V.

config. II, jitter 5 Hz / 0,5 UI

Conformance PASSED

$t_{min} = 0.788022\%$	$t_{max} = 8.788033\%$	$t_{ava} = 8.388015\%$

Measurement finished. Expected TAV-count reached.

V30-11.68b

Input to output offset, short passive bus configuration (high cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with an input sequence of continuous frames with a $2^{19} - 1$ PRBS in D-, D-Echo and both B-channels, restricted power at 32 V.

config. II, jitter 20 Hz / 0,125 UI

Conformance PASSED

$t_{min} = 0.788022\%$	$t_{max} = 8.788033\%$	$t_{ava} = 5.988023\%$

Measurement finished. Expected TAV-count reached.

V30-11.68c

Input to output offset, short passive bus configuration (high cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with an input sequence of continuous frames with a $2^{19}-1$ PRBS in D-, D-Echo and both B-channels, restricted power at 32 V.

config. II, jitter 50 Hz / 0,05 UI

Conformance PASSED

$t_{min} = 0.588020\%$	$t_{max} = 8.588031\%$	$t_{ava} = 7.388022\%$

Measurement finished. Expected TAV-count reached.

V30-11.68d

Input to output offset, short passive bus configuration (high cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with an input sequence of continuous frames with a $2^{19}-1$ PRBS in D-, D-Echo and both B-channels, restricted power at 32 V.

config. II, jitter 2015 Hz / 0,05 UI

Conformance PASSED

$t_{min} = 0.788022\%$	$t_{max} = 8.788033\%$	$t_{ava} = 7.988021\%$

Measurement finished. Expected TAV-count reached.

9.9 Config. IV: Binary ones, different jitter

V30-11.20a

Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with all binary ones in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IV, jitter 5 Hz / 0,5 UI

Conformance PASSED

$t_{min} = 4.238429\%$	$t_{max} = 11.038432\%$	$t_{ava} = 9.038434\%$

Measurement finished. Expected TAV-count reached.

V30-11.20b

Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with all binary ones in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IV, jitter 20 Hz / 0,125 UI

Conformance PASSED

$t_{min} = 4.238429\%$	$t_{max} = 11.038432\%$	$t_{ava} = 9.038434\%$

Measurement finished. Expected TAV-count reached.

V30-11.20c

Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with all binary ones in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IV, jitter 50 Hz / 0,05 UI

Conformance PASSED

$t_{min} = 4.238429\%$	$t_{max} = 11.838422\%$	$t_{ava} = 8.238420\%$

Measurement finished. Expected TAV-count reached.

V30-11.20d

Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with all binary ones in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IV, jitter 2015 Hz / 0,05 UI

Conformance PASSED

$t_{min} = 4.238429\%$	$t_{max} = 11.438427\%$	$t_{ava} = 8.238420\%$

Measurement finished. Expected TAV-count reached.

9.10 Config. IV: Octet 0x0AA, different jitter

V30-11.40a

Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with the octet 0x0AA in both B-channels and binary ones in the D- and D-Echo channels, restricted power at 32 V.

config. IV, jitter 5 Hz / 0,5 UI

Conformance PASSED

$t_{min} = 3.438416\%$	$t_{max} = 11.038432\%$	$t_{ava} = 9.438429\%$

Measurement finished. Expected TAV-count reached.

V30-11.40b

Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with the octet 0x0AA in both B-channels and binary ones in the D- and D-Echo channels, restricted power at 32 V.

config. IV, jitter 20 Hz / 0,125 UI

Conformance PASSED

$t_{min} = 3.438416\%$	$t_{max} = 11.038432\%$	$t_{ava} = 9.038434\%$

Measurement finished. Expected TAV-count reached.

V30-11.40c

Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with the octet 0x0AA in both B-channels and binary ones in the D- and D-Echo channels, restricted power at 32 V.

config. IV, jitter 50 Hz / 0,05 UI

Conformance PASSED

$t_{min} = 3.438416\%$	$t_{max} = 11.038432\%$	$t_{ava} = 10.238419\%$

Measurement finished. Expected TAV-count reached.

V30-11.40d

Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with the octet 0x0AA in both B-channels and binary ones in the D- and D-Echo channels, restricted power at 32 V.

config. IV, jitter 2015 Hz / 0,05 UI

Conformance PASSED

$t_{min} = 4.238429\%$	$t_{max} = 11.038432\%$	$t_{ava} = 7.838426\%$

Measurement finished. Expected TAV-count reached.

9.11 Config. IV: Binary zeros, different jitter

V30-11.60a

Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with all binary zeroes in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IV, jitter 5 Hz / 0,5 UI

Conformance PASSED

$t_{min} = 3.438416\%$	$t_{max} = 11.038432\%$	$t_{ava} = 9.438429\%$

Measurement finished. Expected TAV-count reached.

V30-11.60b

Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with all binary zeroes in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IV, jitter 20 Hz / 0,125 UI

Conformance PASSED

$t_{min} = 4.238429\%$	$t_{max} = 11.038432\%$	$t_{ava} = 9.438429\%$

Measurement finished. Expected TAV-count reached.

V30-11.60c

Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with all binary zeroes in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IV, jitter 50 Hz / 0,05 UI

Conformance PASSED

$t_{min} = 3.438416\%$	$t_{max} = 11.038432\%$	$t_{ava} = 10.238419\%$

Measurement finished. Expected TAV-count reached.

V30-11.60d

Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with all binary zeroes in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IV, jitter 2015 Hz / 0,05 UI

Conformance PASSED

$t_{min} = 3.438416\%$	$t_{max} = 11.438427\%$	$t_{ava} = 7.838426\%$

Measurement finished. Expected TAV-count reached.

9.12 Config. IV: $2^{19} - 1$ PRBS, different jitter

V30-11.80a

Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with a $2^{19} - 1$ PRBS in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IV, jitter 5 Hz / 0,5 UI

Conformance PASSED

$t_{min} = 3.438416\%$	$t_{max} = 11.038432\%$	$t_{ava} = 8.238420\%$

Measurement finished. Expected TAV-count reached.

V30-11.80b

Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with a $2^{19}-1$ PRBS in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IV, jitter 20 Hz / 0,125 UI

Conformance PASSED

$t_{min} = 4.238429\%$	$t_{max} = 11.038432\%$	$t_{ava} = 9.838424\%$

Measurement finished. Expected TAV-count reached.

V30-11.80c

Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with a $2^{19}-1$ PRBS in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IV, jitter 50 Hz / 0,05 UI

Conformance PASSED

$t_{min} = 3.438416\%$	$t_{max} = 11.038432\%$	$t_{ava} = 7.838426\%$

Measurement finished. Expected TAV-count reached.

V30-11.80d

Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with a $2^{19}-1$ PRBS in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IV, jitter 2015 Hz / 0,05 UI

Conformance PASSED

$t_{min} = 3.038421\%$	$t_{max} = 11.038432\%$	$t_{ava} = 9.038434\%$

Measurement finished. Expected TAV-count reached.

9.13 Config. IIIa: Binary ones, different jitter

V30-11.12a

Input to output offset, short passive bus configuration (high cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary ones in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IIIa, jitter 5 Hz / 0,5 UI

Conformance PASSED

$t_{min} = 8.638420\%$	$t_{max} = 11.838422\%$	$t_{ava} = 10.638413\%$

Measurement finished. Expected TAV-count reached.

V30-11.12b

Input to output offset, short passive bus configuration (high cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary ones in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IIIa, jitter 20 Hz / 0,125 UI

Conformance PASSED

$t_{min} = 8.238425\%$	$t_{max} = 11.838422\%$	$t_{ava} = 9.438429\%$

Measurement finished. Expected TAV-count reached.

V30-11.12c

Input to output offset, short passive bus configuration (high cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary ones in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IIIa, jitter 50 Hz / 0,05 UI

Conformance PASSED

$t_{min} = 8.238425\%$	$t_{max} = 11.838422\%$	$t_{ava} = 10.638413\%$

Measurement finished. Expected TAV-count reached.

V30-11.12d

Input to output offset, short passive bus configuration (high cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary ones in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IIIa, jitter 2015 Hz / 0,05 UI

Conformance PASSED

$t_{min} = 3.838434\%$	$t_{max} = 11.838422\%$	$t_{ava} = 10.238419\%$

Measurement finished. Expected TAV-count reached.

9.14 Config. IIIa: Octet 0x0AA, different jitter

V30-11.32a

Input to output offset, short passive bus configuration (high cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with the octet 0x0AA in both B-channels and binary ones in the D- and D-Echo channels, restricted power at 32 V.

config. IIIa, jitter 5 Hz / 0,5 UI

Conformance PASSED

$t_{min} = 7.838430\%$	$t_{max} = 11.038432\%$	$t_{ava} = 10.238419\%$

Measurement finished. Expected TAV-count reached.

V30-11.32b

Input to output offset, short passive bus configuration (high cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with the octet 0x0AA in both B-channels and binary ones in the D- and D-Echo channels, restricted power at 32 V.

config. IIIa, jitter 20 Hz / 0,125 UI

Conformance PASSED

$t_{min} = 8.238425\%$	$t_{max} = 11.838422\%$	$t_{ava} = 9.038434\%$

Measurement finished. Expected TAV-count reached.

V30-11.32c

Input to output offset, short passive bus configuration (high cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with the octet 0x0AA in both B-channels and binary ones in the D- and D-Echo channels, restricted power at 32 V.

config. IIIa, jitter 50 Hz / 0,05 UI

Conformance PASSED

$t_{min} = 8.238425\%$	$t_{max} = 11.838422\%$	$t_{ava} = 9.438429\%$

Measurement finished. Expected TAV-count reached.

V30-11.32d

Input to output offset, short passive bus configuration (high cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with the octet 0x0AA in both B-channels and binary ones in the D- and D-Echo channels, restricted power at 32 V.

config. IIIa, jitter 2015 Hz / 0,05 UI

Conformance PASSED

$t_{min} = 2.238431\%$	$t_{max} = 11.838422\%$	$t_{ava} = 9.038434\%$

Measurement finished. Expected TAV-count reached.

9.15 Config. IIIa: Binary zeros, different jitter

V30-11.52a

Input to output offset, short passive bus configuration (high cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary zeroes in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IIIa, jitter 5 Hz / 0,5 UI

Conformance PASSED

$t_{min} = 8.638420\%$	$t_{max} = 11.838422\%$	$t_{ava} = 9.438429\%$

Measurement finished. Expected TAV-count reached.

V30-11.52b

Input to output offset, short passive bus configuration (high cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary zeroes in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IIIa, jitter 20 Hz / 0,125 UI

Conformance PASSED

$t_{min} = 8.238425\%$	$t_{max} = 11.838422\%$	$t_{ava} = 11.438427\%$

Measurement finished. Expected TAV-count reached.

V30-11.52c

Input to output offset, short passive bus configuration (high cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary zeroes in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IIIa, jitter 50 Hz / 0,05 UI

Conformance PASSED

$t_{min} = 8.238425\%$	$t_{max} = 11.838422\%$	$t_{ava} = 8.638415\%$

Measurement finished. Expected TAV-count reached.

V30-11.52d

Input to output offset, short passive bus configuration (high cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary zeroes in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IIIa, jitter 2015 Hz / 0,05 UI

Conformance PASSED

$t_{min} = 2.238431\%$	$t_{max} = 11.838422\%$	$t_{ava} = 9.438429\%$

Measurement finished. Expected TAV-count reached.

9.16 Config. IIIa: $2^{19} - 1$ PRBS, different jitter

V30-11.72a

Input to output offset, short passive bus configuration (high cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, with the UUT-TE adjacent to the signal source, with an input sequence of continuous frames with a $2^{19} - 1$ PRBS in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IIIa, jitter 5 Hz / 0,5 UI

Conformance PASSED

$t_{min} = 8.638420\%$	$t_{max} = 11.838422\%$	$t_{ava} = 10.638413\%$

Measurement finished. Expected TAV-count reached.

V30-11.72b

Input to output offset, short passive bus configuration (high cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, with the UUT-TE adjacent to the signal source, with an input sequence of continuous frames with a $2^{19} - 1$ PRBS in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IIIa, jitter 20 Hz / 0,125 UI

Conformance PASSED

$t_{min} = 8.238425\%$	$t_{max} = 11.838422\%$	$t_{ava} = 8.638415\%$

Measurement finished. Expected TAV-count reached.

V30-11.72c

Input to output offset, short passive bus configuration (high cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, with the UUT-TE adjacent to the signal source, with an input sequence of continuous frames with a $2^{19} - 1$ PRBS in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IIIa, jitter 50 Hz / 0,05 UI

Conformance PASSED

$t_{min} = 8.238425\%$	$t_{max} = 11.838422\%$	$t_{ava} = 10.238419\%$

Measurement finished. Expected TAV-count reached.

V30-11.72d

Input to output offset, short passive bus configuration (high cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, with the UUT-TE adjacent to the signal source, with an input sequence of continuous frames with a $2^{19} - 1$ PRBS in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IIIa, jitter 2015 Hz / 0,05 UI

Conformance PASSED

$t_{min} = 6.638422\%$	$t_{max} = 11.838422\%$	$t_{ava} = 10.238419\%$

Measurement finished. Expected TAV-count reached.

9.17 Config. IIIb: Binary ones, different jitter

V30-11.16a

Input to output offset, short passive bus configuration (low cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary ones in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IIIb, jitter 5 Hz / 0,5 UI

Conformance PASSED

$t_{min} = 8.638420\%$	$t_{max} = 11.438427\%$	$t_{ava} = 8.638415\%$

Measurement finished. Expected TAV-count reached.

V30-11.16b

Input to output offset, short passive bus configuration (low cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary ones in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IIIb, jitter 20 Hz / 0,125 UI

Conformance PASSED

$t_{min} = 8.238425\%$	$t_{max} = 11.438427\%$	$t_{ava} = 10.238419\%$

Measurement finished. Expected TAV-count reached.

V30-11.16c

Input to output offset, short passive bus configuration (low cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary ones in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IIIb, jitter 50 Hz / 0,05 UI

Conformance PASSED

$t_{min} = 7.838430\%$	$t_{max} = 11.438427\%$	$t_{ava} = 9.038434\%$

Measurement finished. Expected TAV-count reached.

V30-11.16d

Input to output offset, short passive bus configuration (low cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary ones in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IIIb, jitter 2015 Hz / 0,05 UI

Conformance PASSED

$t_{min} = 2.238431\%$	$t_{max} = 11.838422\%$	$t_{ava} = 9.838424\%$

Measurement finished. Expected TAV-count reached.

9.18 Config. IIIb: Octet 0x0AA, different jitter

V30-11.36a

Input to output offset, short passive bus configuration (low cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with the octet 0x0AA in both B-channels and binary ones in the D- and D-Echo channels, restricted power at 32 V.

config. IIIb, jitter 5 Hz / 0,5 UI

Conformance PASSED

$t_{min} = 7.838430\%$	$t_{max} = 11.438427\%$	$t_{ava} = 7.838426\%$

Measurement finished. Expected TAV-count reached.

V30-11.36b

Input to output offset, short passive bus configuration (low cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with the octet 0x0AA in both B-channels and binary ones in the D- and D-Echo channels, restricted power at 32 V.

config. IIIb, jitter 20 Hz / 0,125 UI

Conformance PASSED

$t_{min} = 7.838430\%$	$t_{max} = 11.438427\%$	$t_{ava} = 9.838424\%$

Measurement finished. Expected TAV-count reached.

V30-11.36c

Input to output offset, short passive bus configuration (low cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with the octet 0x0AA in both B-channels and binary ones in the D- and D-Echo channels, restricted power at 32 V.

config. IIIb, jitter 50 Hz / 0,05 UI

Conformance PASSED

$t_{min} = 7.838430\%$	$t_{max} = 11.438427\%$	$t_{ava} = 9.838424\%$

Measurement finished. Expected TAV-count reached.

V30-11.36d

Input to output offset, short passive bus configuration (low cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with the octet 0x0AA in both B-channels and binary ones in the D- and D-Echo channels, restricted power at 32 V.

config. IIIb, jitter 2015 Hz / 0,05 UI

Conformance PASSED

$t_{min} = 6.638422\%$	$t_{max} = 11.838422\%$	$t_{ava} = 7.438431\%$

Measurement finished. Expected TAV-count reached.

9.19 Config. IIIb: Binary zeros, different jitter

V30-11.56a

Input to output offset, short passive bus configuration (low cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary zeroes in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IIIb, jitter 5 Hz / 0,5 UI

Conformance PASSED

$t_{min} = 8.238425\%$	$t_{max} = 11.438427\%$	$t_{ava} = 8.638415\%$

Measurement finished. Expected TAV-count reached.

V30-11.56b

Input to output offset, short passive bus configuration (low cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary zeroes in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IIIb, jitter 20 Hz / 0,125 UI

Conformance PASSED

$t_{min} = 7.838430\%$	$t_{max} = 11.438427\%$	$t_{ava} = 9.038434\%$

Measurement finished. Expected TAV-count reached.

V30-11.56c

Input to output offset, short passive bus configuration (low cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary zeroes in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IIIb, jitter 50 Hz / 0,05 UI

Conformance PASSED

$t_{min} = 7.838430\%$	$t_{max} = 11.438427\%$	$t_{ava} = 10.238419\%$

Measurement finished. Expected TAV-count reached.

V30-11.56d

Input to output offset, short passive bus configuration (low cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary zeroes in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IIIb, jitter 2015 Hz / 0,05 UI

Conformance PASSED

$t_{min} = 6.638422\%$	$t_{max} = 11.838422\%$	$t_{ava} = 9.038434\%$

Measurement finished. Expected TAV-count reached.

9.20 Config. IIIb: $2^{19} - 1$ PRBS, different jitter

V30-11.76a

Input to output offset, short passive bus configuration (low cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, with the UUT-TE adjacent to the signal source, with an input sequence of continuous frames with a $2^{19} - 1$ PRBS in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IIIb, jitter 5 Hz / 0,5 UI

Conformance PASSED

$t_{min} = 8.638420\%$	$t_{max} = 11.438427\%$	$t_{ava} = 9.838424\%$

Measurement finished. Expected TAV-count reached.

V30-11.76b

Input to output offset, short passive bus configuration (low cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, with the UUT-TE adjacent to the signal source, with an input sequence of continuous frames with a $2^{19} - 1$ PRBS in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IIIb, jitter 20 Hz / 0,125 UI

Conformance PASSED

$t_{min} = 7.838430\%$	$t_{max} = 11.438427\%$	$t_{ava} = 11.038432\%$

Measurement finished. Expected TAV-count reached.

V30-11.76c

Input to output offset, short passive bus configuration (low cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, with the UUT-TE adjacent to the signal source, with an input sequence of continuous frames with a $2^{19} - 1$ PRBS in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IIIb, jitter 50 Hz / 0,05 UI

Conformance PASSED

$t_{min} = 7.838430\%$	$t_{max} = 11.438427\%$	$t_{ava} = 9.838424\%$

Measurement finished. Expected TAV-count reached.

V30-11.76d

Input to output offset, short passive bus configuration (low cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, with the UUT-TE adjacent to the signal source, with an input sequence of continuous frames with a $2^{19} - 1$ PRBS in D-, D-Echo and both B-channels, restricted power at 32 V.

config. IIIb, jitter 2015 Hz / 0,05 UI

Conformance PASSED

$t_{min} = 2.238431\%$	$t_{max} = 11.838422\%$	$t_{ava} = 9.438429\%$

Measurement finished. Expected TAV-count reached.

10 Receiver sensitivity

10.1 config. IIIa: 1.5 dB attenuated, different jitter

V30-17.20a

Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5 dB attenuated signal source, restricted power at 32 V.

config. IIIa, jitter 5 Hz / 0,5 UI

Conformance PASSED

Intervals = 1	Bit Error Count = 0.000000
Errored Intervals = 0	Bit Error Rate = 0.000000
Time = 60.000000 s	

V30-17.20b

Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5 dB attenuated signal source, restricted power at 32 V.

config. IIIa, jitter 20 Hz / 0,125 UI

Conformance PASSED

V30-17.20c

Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5 dB attenuated signal source, restricted power at 32 V.

config. IIIa, jitter 50 Hz / 0,05 UI

Conformance PASSED

V30-17.20d

Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5 dB attenuated signal source, restricted power at 32 V.

config. IIIa, jitter 2015 Hz / 0,05 UI

Conformance PASSED

10.2 config. IIIa: 1.5 dB gain, different jitter

V30-17.24a

Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5 dB gain signal source, restricted power at 32 V.

config. IIIa, jitter 5 Hz / 0,5 UI

Conformance PASSED

V30-17.24b

Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5 dB gain signal source, restricted power at 32 V.

config. IIIa, jitter 20 Hz / 0,125 UI

Conformance PASSED

V30-17.24c

Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5 dB gain signal source, restricted power at 32 V.

config. IIIa, jitter 50 Hz / 0,05 UI

Conformance PASSED

V30-17.24d

Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5 dB gain signal source, restricted power at 32 V.

config. IIIa, jitter 2015 Hz / 0,05 UI

Conformance PASSED

10.3 config. IIIb: 1.5 dB attenuated, different jitter

V30-17.28a

Receiver sensitivity with jitter, short passive bus configuration (low cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with a 1.5 dB attenuated signal source, restricted power at 32 V.

config. IIIb, jitter 5 Hz / 0,5 UI

Conformance PASSED

V30-17.28b

Receiver sensitivity with jitter, short passive bus configuration (low cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with a 1.5 dB attenuated signal source, restricted power at 32 V.

config. IIIb, jitter 20 Hz / 0,125 UI

Conformance PASSED

V30-17.28c

Receiver sensitivity with jitter, short passive bus configuration (low cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with a 1.5 dB attenuated signal source, restricted power at 32 V.

config. IIIb, jitter 50 Hz / 0,05 UI

Conformance PASSED

V30-17.28d

Receiver sensitivity with jitter, short passive bus configuration (low cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with a 1.5 dB attenuated signal source, restricted power at 32 V.

config. IIIb, jitter 2015 Hz / 0,05 UI

Conformance PASSED

10.4 config. IIIb: 1.5 dB gain, different jitter

V30-17.32a

Receiver sensitivity with jitter, short passive bus configuration (low cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with a 1.5 dB gain signal source, restricted power at 32 V.

config. IIIb, jitter 5 Hz / 0,5 UI

Conformance PASSED

V30-17.32b

Receiver sensitivity with jitter, short passive bus configuration (low cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with a 1.5 dB gain signal source, restricted power at 32 V.

config. IIIb, jitter 20 Hz / 0,125 UI

Conformance PASSED

V30-17.32c

Receiver sensitivity with jitter, short passive bus configuration (low cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with a 1.5 dB gain signal source, restricted power at 32 V.

config. IIIb, jitter 50 Hz / 0,05 UI

Conformance PASSED

V30-17.32d

Receiver sensitivity with jitter, short passive bus configuration (low cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with a 1.5 dB gain signal source, restricted power at 32 V.

config. IIIb, jitter 2015 Hz / 0,05 UI

Conformance PASSED

10.5 config. I: 1.5 dB attenuated, 200 kHz noise, different jitter

V30-17.4a

Receiver sensitivity with 200 kHz sine wave noise and jitter, short point to point configuration (high cap. cable with 6 dB attenuation) with a with a 1.5 dB attenuated signal source, restricted power at 32 V.

config. I, jitter 5 Hz / 0,5 UI

Conformance PASSED

V30-17.4b

Receiver sensitivity with 200 kHz sine wave noise and jitter, short point to point configuration (high cap. cable with 6 dB attenuation) with a with a 1.5 dB attenuated signal source, restricted power at 32 V.

config. I, jitter 20 Hz / 0,125 UI

Conformance PASSED

V30-17.4c

Receiver sensitivity with 200 kHz sine wave noise and jitter, short point to point configuration (high cap. cable with 6 dB attenuation) with a with a 1.5 dB attenuated signal source, restricted power at 32 V.

config. I, jitter 50 Hz / 0,05 UI

Conformance PASSED

V30-17.4d

Receiver sensitivity with 200 kHz sine wave noise and jitter, short point to point configuration (high cap. cable with 6 dB attenuation) with a with a 1.5 dB attenuated signal source, restricted power at 32 V.

config. I, jitter 2015 Hz / 0,05 UI

Conformance PASSED

10.6 config. I: 1.5 dB attenuated, 2 MHz noise, different jitter

V30-17.8a

Receiver sensitivity with 2 MHz sine wave noise and jitter, short point to point configuration (high cap. cable with 6 dB attenuation) with a with a 1.5 dB attenuated signal source, restricted power at 32 V.

config. I, jitter 5 Hz / 0,5 UI

Conformance PASSED

V30-17.8b

Receiver sensitivity with 2 MHz sine wave noise and jitter, short point to point configuration (high cap. cable with 6 dB attenuation) with a with a 1.5 dB attenuated signal source, restricted power at 32 V.

config. I, jitter 20 Hz / 0,125 UI

Conformance PASSED

V30-17.8c

Receiver sensitivity with 2 MHz sine wave noise and jitter, short point to point configuration (high cap. cable with 6 dB attenuation) with a with a 1.5 dB attenuated signal source, restricted power at 32 V.

config. I, jitter 50 Hz / 0,05 UI

Conformance PASSED

V30-17.8d

Receiver sensitivity with 2 MHz sine wave noise and jitter, short point to point configuration (high cap. cable with 6 dB attenuation) with a with a 1.5 dB attenuated signal source, restricted power at 32 V.

config. I, jitter 2015 Hz / 0,05 UI

Conformance PASSED

10.7 config. II: 1.5 dB attenuated, different jitter

V30-17.12a

Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5 dB attenuated signal source, restricted power at 32 V.

config. II, jitter 5 Hz / 0,5 UI

Conformance PASSED

V30-17.12b

Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5 dB attenuated signal source, restricted power at 32 V.

config. II, jitter 20 Hz / 0,125 UI

Conformance PASSED

V30-17.12c

Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5 dB attenuated signal source, restricted power at 32 V.

config. II, jitter 50 Hz / 0,05 UI

Conformance PASSED

V30-17.12d

Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5 dB attenuated signal source, restricted power at 32 V.

config. II, jitter 2015 Hz / 0,05 UI

Conformance PASSED

10.8 config. II: 1.5 dB gain, different jitter

V30-17.16a

Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5 dB gain signal source, restricted power at 32 V.

config. II, jitter 5 Hz / 0,5 UI

Conformance PASSED

V30-17.16b

Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5 dB gain signal source, restricted power at 32 V.

config. II, jitter 20 Hz / 0,125 UI

Conformance PASSED

V30-17.16c

Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5 dB gain signal source, restricted power at 32 V.

config. II, jitter 50 Hz / 0,05 UI

Conformance PASSED

V30-17.16d

Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5 dB gain signal source, restricted power at 32 V.

config. II, jitter 2015 Hz / 0,05 UI

Conformance PASSED

10.9 config. IV: 1.5 dB gain, different jitter

V30-17.36a

Receiver sensitivity with jitter, ideal configuration (direct connection UUT-TE to NT) with a 1.5 dB gain signal source, restricted power at 32 V.

config. IV, jitter 5 Hz / 0,5 UI

Conformance PASSED

V30-17.36b

Receiver sensitivity with jitter, ideal configuration (direct connection UUT-TE to NT) with a 1.5 dB gain signal source, restricted power at 32 V.

config. IV, jitter 20 Hz / 0,125 UI

Conformance PASSED

V30-17.36c

Receiver sensitivity with jitter, ideal configuration (direct connection UUT-TE to NT) with a 1.5 dB gain signal source, restricted power at 32 V.

config. IV, jitter 50 Hz / 0,05 UI

Conformance PASSED

V30-17.36d

Receiver sensitivity with jitter, ideal configuration (direct connection UUT-TE to NT) with a 1.5 dB gain signal source, restricted power at 32 V.

config. IV, jitter 2015 Hz / 0,05 UI

Conformance PASSED

11 Jitter characteristics

11.1 Config. I: Different input sequences

V30-10.4

Jitter characteristics when transmitting INFO 3, point to point configuration (high cap. cable with 6 dB attenuation) with an input sequence of continuous frames with all binary ones in D-, D-Echo and both B-channels, restricted power at 32 V.

Weighted and spectral, config. I, +basic unit: Peak to peak

$UI(pp) = 6.300000\%$	$UI(rms) = 0.800000\%$	$UI(pp-Hold) = 6.500000\%$

Measurement finished. Expected TAV-count reached.

V30-10.24

Jitter characteristics when transmitting INFO 3, point to point configuration (high cap. cable with 6 dB attenuation) with an input sequence of 40 frames with continuous octets of 0x0AA in both B-channels an continuous ones in the D- and D-Echo channels followed by 40 frames with continuous binary zeroes in D-, D-Echo and both B-channels, restricted power at 32 V.

Weighted and spectral, config. I, +basic unit: Peak to peak

$UI(pp) = 4.500000\%$	$UI(rms) = 0.700000\%$	$UI(pp-Hold) = 4.500000\%$

Measurement finished. Expected TAV-count reached.

V30-10.44

Jitter characteristics when transmitting INFO 3, point to point configuration (high cap. cable with 6 dB attenuation) with an input sequence of continuous frames with a $2^{19} - 1$ PRBS in D-, D-Echo and both B-channels, restricted power at 32 V.

Weighted and spectral, config. I, +basic unit: Peak to peak

$UI(pp) = 7.400000\%$	$UI(rms) = 1.100000\%$	$UI(pp-Hold) = 7.800000\%$

Measurement finished. Expected TAV-count reached.

11.2 Config. II: Different input sequences

V30-10.8

Jitter characteristics when transmitting INFO 3,

short passive bus configuration (high cap. cable with 2 μs delay)with 8 TEs (including the UUT-TE) clustered at the far end of the bus with an input sequence of continuous frames with all binary ones in D-, D-Echo and both B-channels, restricted power at 32 V.

Weighted and spectral, config. II, +basic unit: Peak to peak

$UI(pp) = 5.000000\%$	$UI(rms) = 0.800000\%$	$UI(pp-Hold) = 5.100000\%$

Measurement finished. Expected TAV-count reached.

V30-10.28

Jitter characteristics when transmitting INFO 3, short passive bus configuration (high cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus, with an input sequence of 40 frames with continuous octets of 0x0AA in both B-channels an continuous ones in the D- and D-Echo channels followed by 40 frames with continuous binary zeroes in D-, D-Echo and both B-channels, restricted power at 32 V.

Weighted and spectral, config. II, +basic unit: Peak to peak

$UI(pp) = 4.800000\%$	$UI(rms) = 0.700000\%$	$UI(pp-Hold) = 4.800000\%$

Measurement finished. Expected TAV-count reached.

V30-10.48

Jitter characteristics when transmitting INFO 3, short passive bus configuration (high cap. cable with 2 μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with an input sequence of continuous frames with a $2^{19}-1$ PRBS in D-, D-Echo and both B-channels, restricted power at 32 V.

Weighted and spectral, config. II, +basic unit: Peak to peak

$UI(pp) = 5.500000\%$	$UI(rms) = 0.900000\%$	$UI(pp-Hold) = 5.900000\%$

Measurement finished. Expected TAV-count reached.

11.3 Config. IV: Different input sequences

V30-10.20

Jitter characteristics when transmitting INFO 3, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with all binary ones in D-, D-Echo and both B-channels, restricted power at 32 V.

Weighted and spectral, config. IV, +basic unit: Peak to peak

$UI(pp) = 4.600000\%$	$UI(rms) = 0.900000\%$	$UI(pp-Hold) = 4.600000\%$

Measurement finished. Expected TAV-count reached.

V30-10.40

Jitter characteristics when transmitting INFO 3, ideal configuration (direct connection TE to NT) with an input sequence of 40 frames with continuous octets of 0x0AA in both B-channels an continuous ones in the D- and D-Echo channels followed by 40 frames with continuous binary zeroes in D-, D-Echo and both B-channels, restricted power at 32 V.

Weighted and spectral, config. IV, basic unit: Peak to peak

$UI(pp) = 4.600000\%$	$UI(rms) = 0.800000\%$	$UI(pp-Hold) = 4.700000\%$

Measurement finished. Expected TAV-count reached.

V30-10.60

Jitter characteristics when transmitting INFO 3, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with a $2^{19}-1$ PRBS in D-, D-Echo and both B-channels, restricted power at 32 V.

Weighted and spectral, config. IV, basic unit: Peak to peak

$UI(pp) = 4.900000\%$	$UI(rms) = 0.900000\%$	$UI(pp-Hold) = 5.000000\%$

Measurement finished. Expected TAV-count reached.

11.4 Config. IIIa: Different input sequences

V30-10.12

Jitter characteristics when transmitting INFO 3, short passive bus configuration (high cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary ones in D-, D-Echo and both B-channels, restricted power at 32 V.

Weighted and spectral, config. IIIa, +basic unit: Peak to peak

$UI(pp) = 5.100000\%$	$UI(rms) = 0.800000\%$	$UI(pp-Hold) = 5.200000\%$

Measurement finished. Expected TAV-count reached.

V30-10.32

Jitter characteristics when transmitting INFO 3, short passive bus configuration (high cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of 40 frames with continuous octets of 0x0AA in both B-channels an continuous ones in the D- and D-Echo channels followed by 40 frames with continuous binary zeroes in D-, D-Echo and both B-channels, restricted power at 32 V.

Weighted and spectral, config. IIIa, +basic unit: Peak to peak

$UI(pp) = 4.700000\%$	$UI(rms) = 0.700000\%$	$UI(pp-Hold) = 4.900000\%$

Measurement finished. Expected TAV-count reached.

V30-10.52

Jitter characteristics when transmitting INFO 3, short passive bus configuration (high cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, with the UUT-TE adjacent to the signal source, with an input sequence of continuous frames with a $2^{19}-1$ PRBS in D-, D-Echo and both B-channels, restricted power at 32 V.

Weighted and spectral, config. IIIa, +basic unit: Peak to peak

$UI(pp) = 5.600000\%$	$UI(rms) = 0.900000\%$	$UI(pp-Hold) = 5.800000\%$

Measurement finished. Expected TAV-count reached.

11.5 Config. IIIb: Different input sequences

V30-10.16

Jitter characteristics when transmitting INFO 3, short passive bus configuration (low cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary ones in D-, D-Echo and both B-channels, restricted power at 32 V.

Weighted and spectral, config. IIIb, +basic unit: Peak to peak

$UI(pp) = 5.200000\%$	$UI(rms) = 0.800000\%$	$UI(pp-Hold) = 5.200000\%$

Measurement finished. Expected TAV-count reached.

V30-10.36

Jitter characteristics when transmitting INFO 3, short passive bus configuration (low cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of 40 frames with continuous octets of 0x0AA in both B-channels an continuous ones in the D- and D-Echo channels followed by 40 frames with continiuous binary zeroes in D-, -Echo and both B-channels, restricted power at 32 V.

Weighted and spectral, config. IIIb, +basic unit: Peak to peak

$UI(pp) = 5.200000\%$	$UI(rms) = 0.700000\%$	$UI(pp-Hold) = 5.200000\%$

Measurement finished. Expected TAV-count reached.

V30-10.56

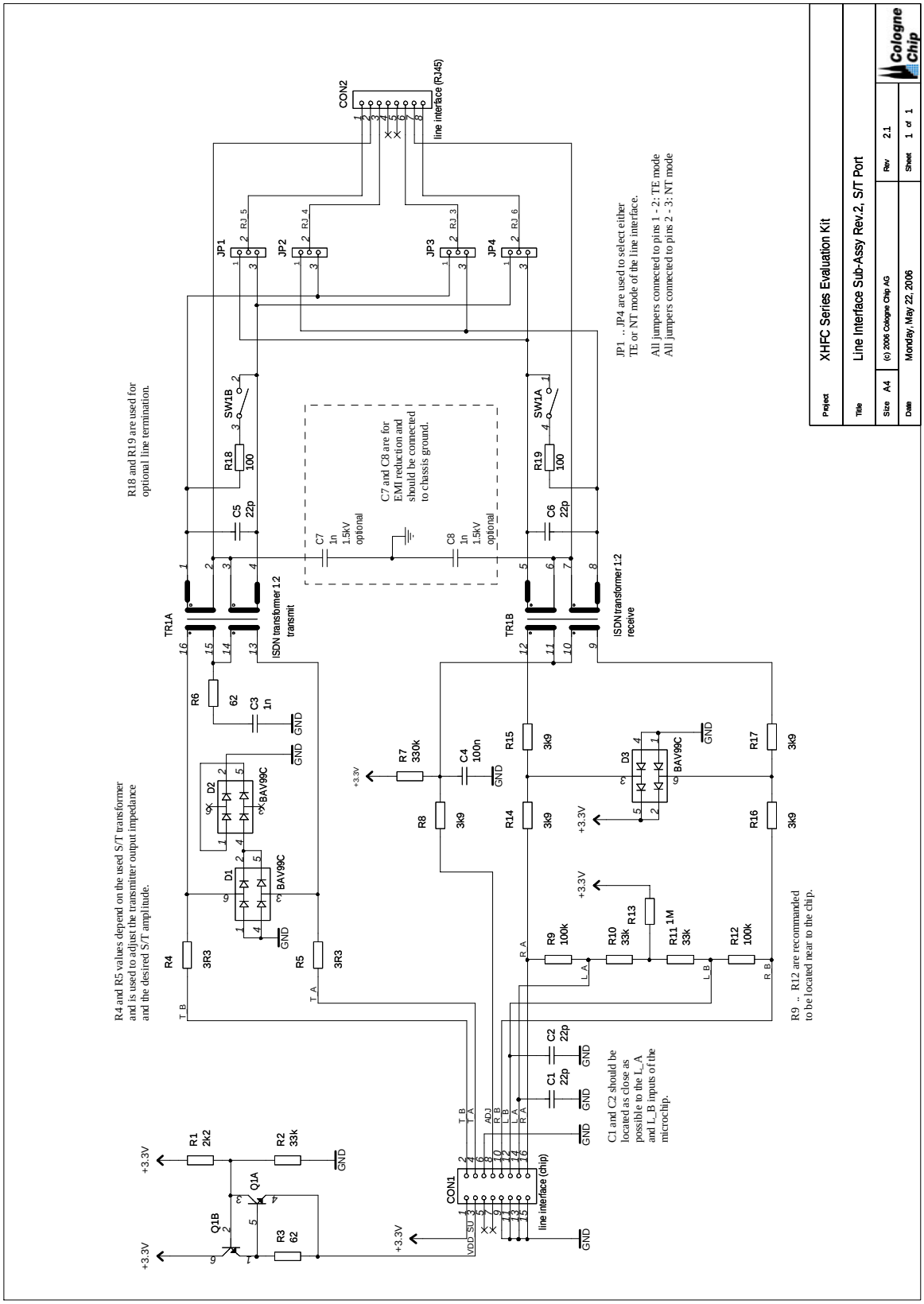
Jitter characteristics when transmitting INFO 3, short passive bus configuration (low cap. cable with 2 μs delay) with 7 TEs clustered at the far end of the bus, with the UUT-TE adjacent to the signal source, with an input sequence of continuous frames with a $2^{19}-1$ PRBS in D-, D-Echo and both B-channels, restricted power at 32 V.

weighted and spectral, config. IIIb, +basic unit: Peak to peak

$UI(pp) = 5.400000\%$	$UI(rms) = 0.900000\%$	$UI(pp-Hold) = 5.500000\%$

Measurement finished. Expected TAV-count reached.

A S/T line interface schematic



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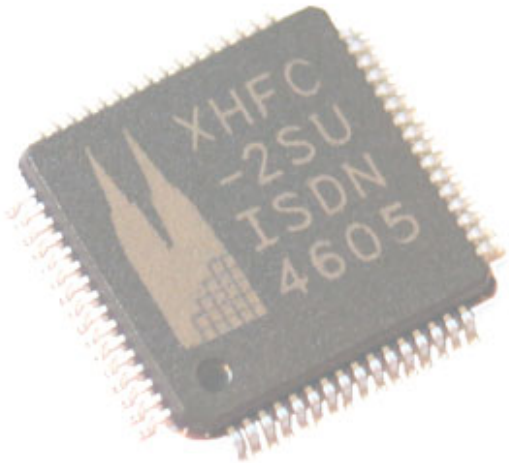

Cologne Chip AG

Test Report