

# XHFC Series Evaluation Kit

## XHFC - 1SU Evaluation Board Revision 1

### Hardware Description

January 2016

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# 1 Overview

XHFC-1SU is a single-chip ISDN transceiver with integrated HDLC controller for one ISDN S/T or  $U_{pN} / U_{p0}$ <sup>1</sup> Basic Rate Interface. Similar microchips with two ISDN ports or with four ISDN ports are also available within the XHFC microchip series.

This document describes the XHFC-1SU Evaluation Board revision 1 which is part of the XHFC Series Evaluation Kit. Different line interface subassemblies are available and must be piggybacked onto the XHFC-1SU Evaluation Board.

The XHFC-1SU Evaluation Board is made of the following functional parts:

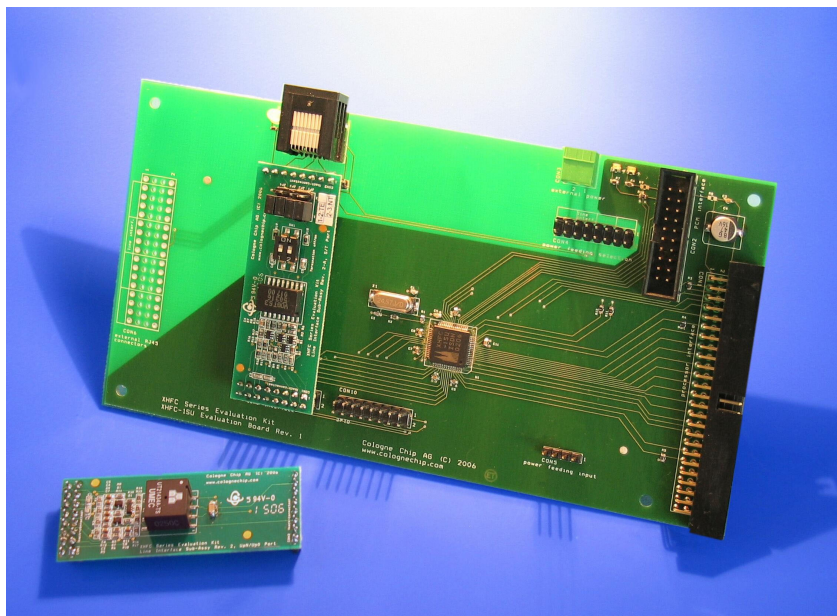
- the XHFC-1SU microchip
- a socket to mount a line interface subassembly
- a socket for a power feeding module (optional)
- a connector to the host processor system
- a PCM interface connector

The schematic is shown in Figures 3 and 4 from page 7.

The printed circuit board consists of 4 layers. Signal traces are assigned to the outer layers while the inner layers are used for ground and power planes. Views of the board design are shown in Figures 5 to 7 from page 10.

Please refer to the data sheet [1] for detailed information on the XHFC-1SU microchip.

Software is not included in the XHFC Series Evaluation Kit. Please contact the Cologne Chip support team for a demo layer 1 driver, register header files, Linux drivers or further software support.



**Figure 1:** XHFC-1SU Evaluation Board with a subassembly for S/T line interface mounted and an additional subassembly for  $U_{pN} / U_{p0}$  line interface beside

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<sup>1</sup> $U_{pN} / U_{p0}$  in the following referred to as  $U_p$ .

## 2 Evaluation board description

### 2.1 Line interfaces

The XHFC-1SU Evaluation Board has a board socket CON7/CON8 to piggyback a line interface module.

Several line interface subassemblies can be used with the XHFC Series Evaluation Kit:

- Line Interface Subassembly for S/T Port (universal circuitry for TE mode and NT mode) [2]
- Line Interface Subassembly for S/T Port (reduced circuitry for NT mode only) [3]
- Line Interface Subassembly for S/T Port with software configuration (TE/NT mode selection, line termination and power feeding enable / disable) [4]
- Line Interface Subassembly for  $U_{pN}$  /  $U_{p0}$  Port [5]
- Line Interface Subassembly for combined ST/ $U_p$  Port (same circuitry can be used for either S/T or  $U_{pN}$  /  $U_{p0}$  mode selected by coding plug) [6]
- Line Interface Subassembly for combined ST/ $U_p$  Port (same circuitry can be used for either S/T or  $U_{pN}$  /  $U_{p0}$  mode detected automatically) [7]

For every XHFC Series Evaluation Kit order, the Cologne Chip team asserts a set of subassemblies according to the specific project requirements.

A RJ45 jack for the line interface is mounted on the XHFC-1SU Evaluation Board.

An optional connector to pass the line interface signal to an external system in replacement for the RJ45 jack is provided as well.

### 2.2 Power feeding

The line interface can have power feeding capability. Power feeding is an option for bus-powered terminal devices, e.g. phones, and must not be enabled for terminals in TE mode.

Two different operation modes can be used as described in the following.

#### External power feeding source

The external power source has to be connected to CON3. The typical voltage range is 34 V .. 42 V.

Jumpers on CON4 are used to enable power feeding of the line interface. Two jumpers are required on pins 9 – 11 (P-) and pins 10 – 12 (P+). Without jumpers inserted, the power source is not connected to the line interface.

CON5 is not used in this operation mode.

#### Using the power feeding module on board socket CON4/CON5 (optional)

An optional power feeding module can be piggybacked onto the board socket CON4/CON5. It generates 38 V from 12 V input voltage connected to CON3.

## 2.3 General purpose I/O signals

Six GPIO signals GPIO12..GPIO15, GPIO18 and GPIO19 from XHFC-1SU are accessible at connector CON10.

Two further GPIO signals at CON10, GP1\_0 (GPIO2) and GP1\_1 (GPIO3), are available but are shared with signals at the PCM interface connector (see section 2.4).

Two additional GPIO signals on CON7, GP0\_0 and GP0\_1, are provided for service bits on the line interface subassembly and are unreserved when the subassembly is not mounted on the board socket. As some line interface subassemblies do not use their GPIO signals, these can be used for other purposes optionally. Please refer to the subassembly documentations [2, 5].

## 2.4 PCM interface

The PCM interface and several additional signals are wired to CON2. The connection to an external PCM bus and to synchronization signals can be configured with  $0\Omega$  resistors R9..12 which are optionally populated or omitted due to the application needs.

Furthermore, F1\_0 and F1\_1 signals or their second pin functions GPIO2 and GPIO3 of XHFC-1SU can be used for three different tasks on the XHFC-1SU Evaluation Board:

1. Two LEDs D1 and D2 can report status information on GPIO2 and GPIO3 outputs.
2. F1\_0 and F1\_1 can be wired to CON2 with R9 and R10 populated. These signals can be used for external CODECs connected to the PCM bus, e.g.
3. GPIO2 and GPIO3 can be used at the GPIO connector CON10.

## 2.5 Host processor interface

The host processor has to be connected to CON1. As all XHFC-1SU pins of the microprocessor interface are wired to CON1, all processor modes can be used with the XHFC-1SU Evaluation Board:

- Serial processor interface (SPI)
- Parallel processor interface in Motorola mode (8 bit, multiplexed)
- Parallel processor interface in Motorola mode (8 bit, non-multiplexed)
- Parallel processor interface in Siemens / Intel mode (8 bit, multiplexed)
- Parallel processor interface in Siemens / Intel mode (8 bit, non-multiplexed)

Figure 2 shows how to interconnect the XHFC-1SU Evaluation Board to an SPI system. CON100 has to be connected to CON1 of the XHFC-1SU Evaluation Board. Please note, that all signal names at CON100 are changed to SPI pin names of the XHFC-1SU. Pins 21, 23 and 39 of CON100 must not be connected. All other open pins (1, 2, 6, even numbers 10 .. 46, 49) are attached to ground or power supply of the XHFC-1SU Evaluation Board.

For interconnection of the XHFC-1SU Evaluation Board to a parallel processor system, please refer to the data sheet schematics [1].



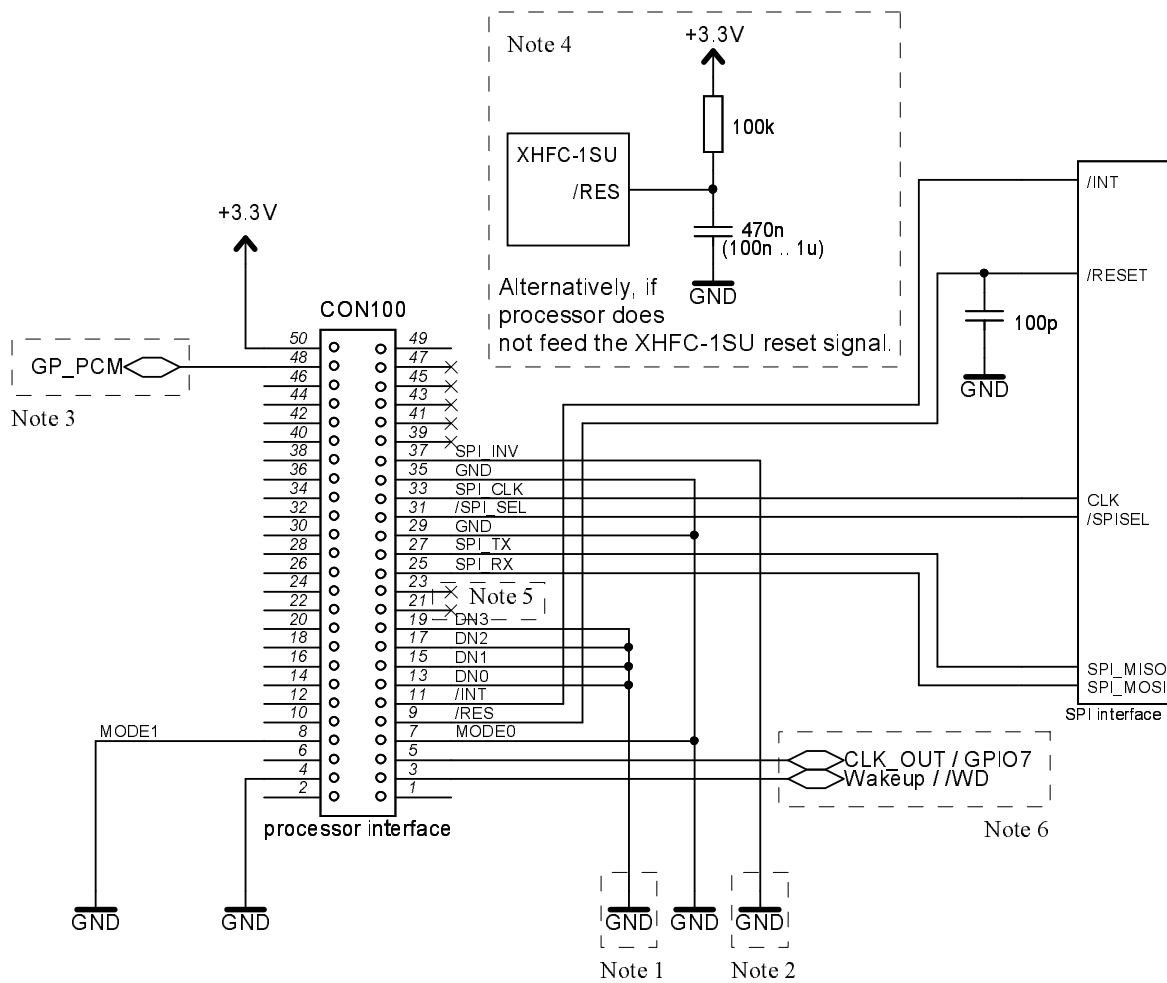
### **Please note !**

Please note, that pins 35 and 29 of CON100 must be connected to ground in SPI mode. These pins have a different function in parallel processor mode. Thus, ground connection via any GND pin (4, 6 or even numbers 10 .. 46) is required as well.

Pins 23, 21 and 39 of CON100 are NC in SPI mode and must not be connected. They are only used in parallel processor mode.

## 2.6 Power supply

The XHFC-1SU Evaluation Board requires 3.3 V stabilized supply voltage on CON1 pins 1, 2, 49 and 50. System ground must be connected to CON1 pins 4, 6 and others (please refer to the schematic on page 7).



Note 1:

DN0 .. 3 are used to select an SPI device number. Any number in the range 0 .. 15 is allowed and '0000' is shown here.

Note 2:

SPI\_INV can optionally be used to invert the SPI clock. It should either be connected to ground or power supply.

Note 3:

GP\_PCM can optionally be used to offer a GPIO signal to the PCM connector of the XHFC Series Evaluation Kit. It can be left open if not used.

**Important note:**

**DN0 .. 3 can only be connected to VDD or GND when MODE0 and MODE1 pins are fixed to GND. Otherwise serial resistors must be inserted because DN0 ..3 might be outputs during reset.**

Note 4:

The reset pin /RES of XHFC-1SU should never be left open. See data sheet for detailed reset information.

Note 5:

XHFC-1SU pins 6 and 7 (CON1 pins 21 and 23) should be connected to ground in SPI mode to avoid floating inputs.

However, the SPI connection of the eval board leaves them open to avoid short circuit if XHFC-1SU is in parallel processor mode during start-up procedure.

Note 6:

These signals can optionally be used. When not used, they should be configured to output characteristic and can be left open in this case.

**Figure 2:** XHFC-1SU Evaluation Board interconnection to an SPI system

### 3 Evaluation board schematic

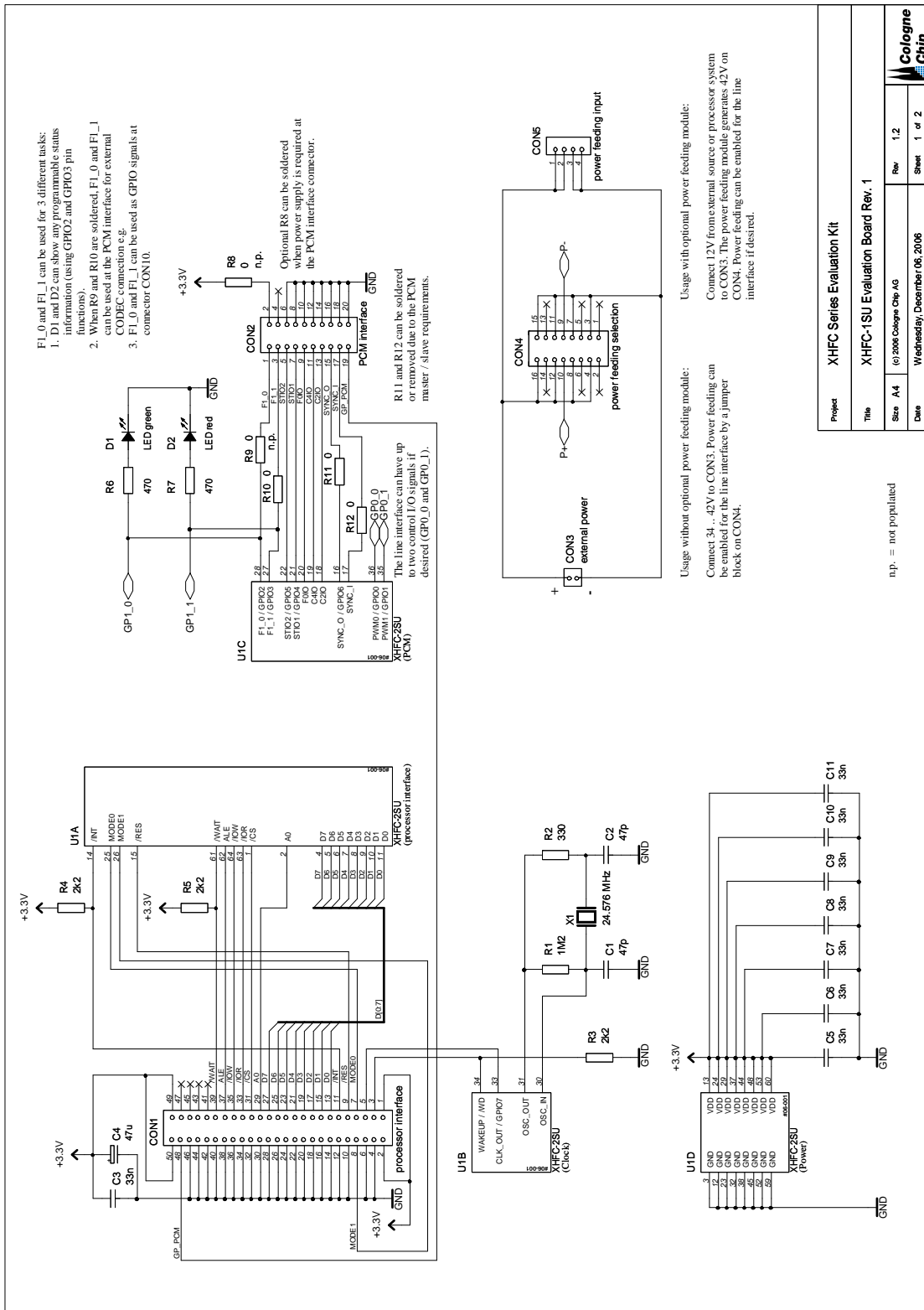


Figure 3: XHFC-1SU Evaluation Board schematic (page 1 of 2)

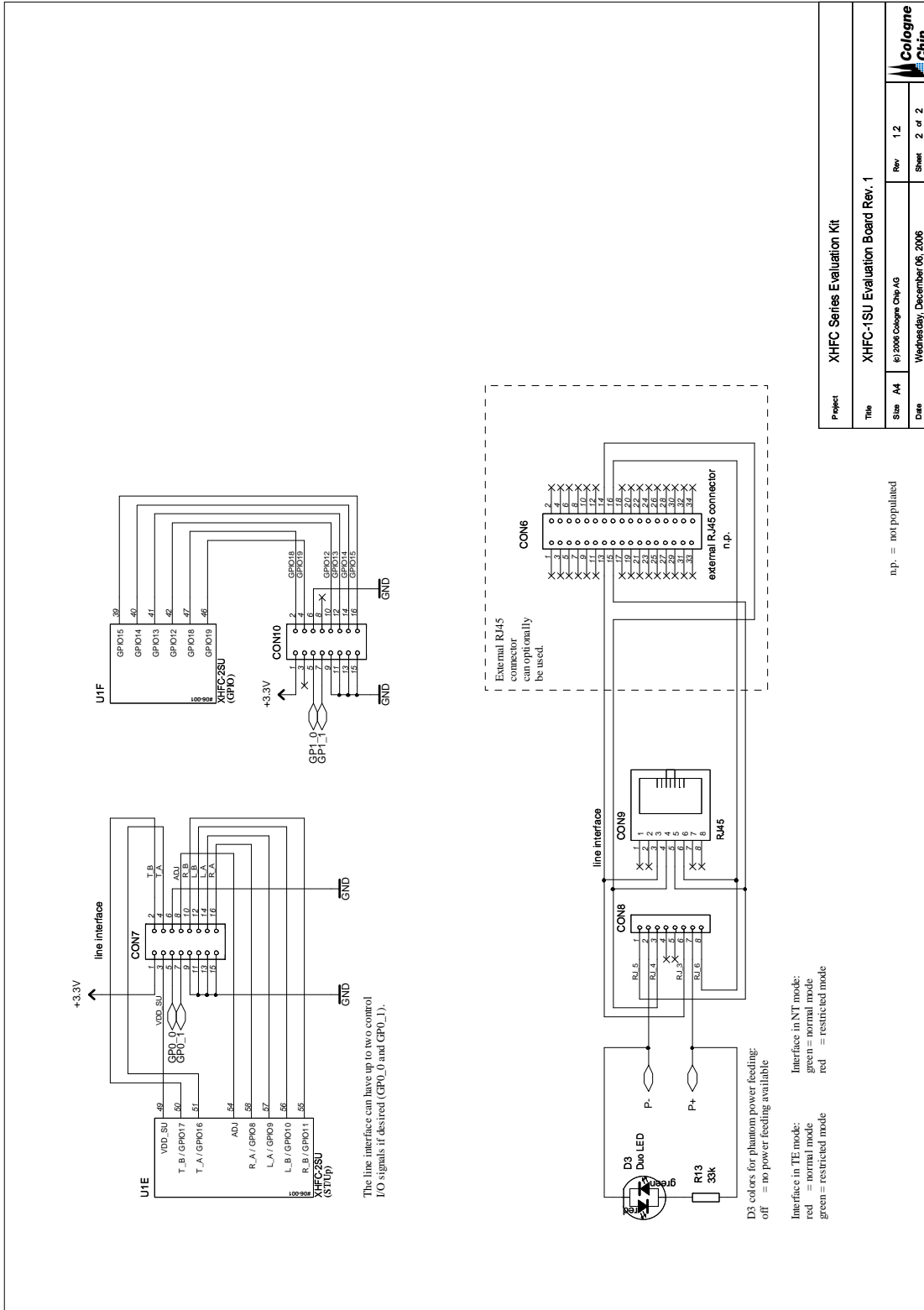


Figure 4: XHFC-1SU Evaluation Board schematic (page 2 of 2)

Project	XHFC Series Evaluation Kit		
Title	XHFC-1SU Evaluation Board Rev. 1		
Size	A4	Rev	1.2
Date	© 2008 Cologne Chip AG Wednesday, December 06, 2006		Sheet 2 of 2



**Bill of Materials: XHFC Series Evaluation Kit**  
**XHFC-1SU Evaluation Board Rev. 1**

Revision: 1.2, generated on Wednesday, December 06, 2006 by Cologne Chip AG

(n.p. = not populated)

**Resistors (11..13 pcs.)**

R1	1M	
R2	330	
R3,R4,R5	2k2	
R6,R7	470	
R8,R9	0	n.p.
R10,R11,R12	0	
R13	33k	

**Capacitors (11 pcs.)**

C1,C2	47p
C3,C5,C6,C7,C8,C9,C10,C11	33n
C4	47u

**Diodes (3 pcs.)**

D1	LED green
D2	LED red
D3	Duo LED

**Integrated Circuits (ICs) (1 pc.)**

U1	XHFC-1SU
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**Connectors (9..10 pcs.)**

CON1	Box header 2x25, angled
CON2	Box header 2x10
CON3	STL1550-2-G35-H
CON4,CON7,CON10	Pin header 2x8
CON5	Pin header 1x4
CON6	Female header 2x17, dual entry type
CON8	Pin header 1x8
CON9	RJ45

**Oscillators (1 pcs.)**

X1	24.576 MHz
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**Total:**

- 11 x Resistors
- 11 x Capacitors
- 3 x Diodes
- 1 x Integrated Circuits (ICs)
- 9 x Connectors
- 1 x Oscillators

36 total  
+ 3 not populated

## 4 Evaluation board layout

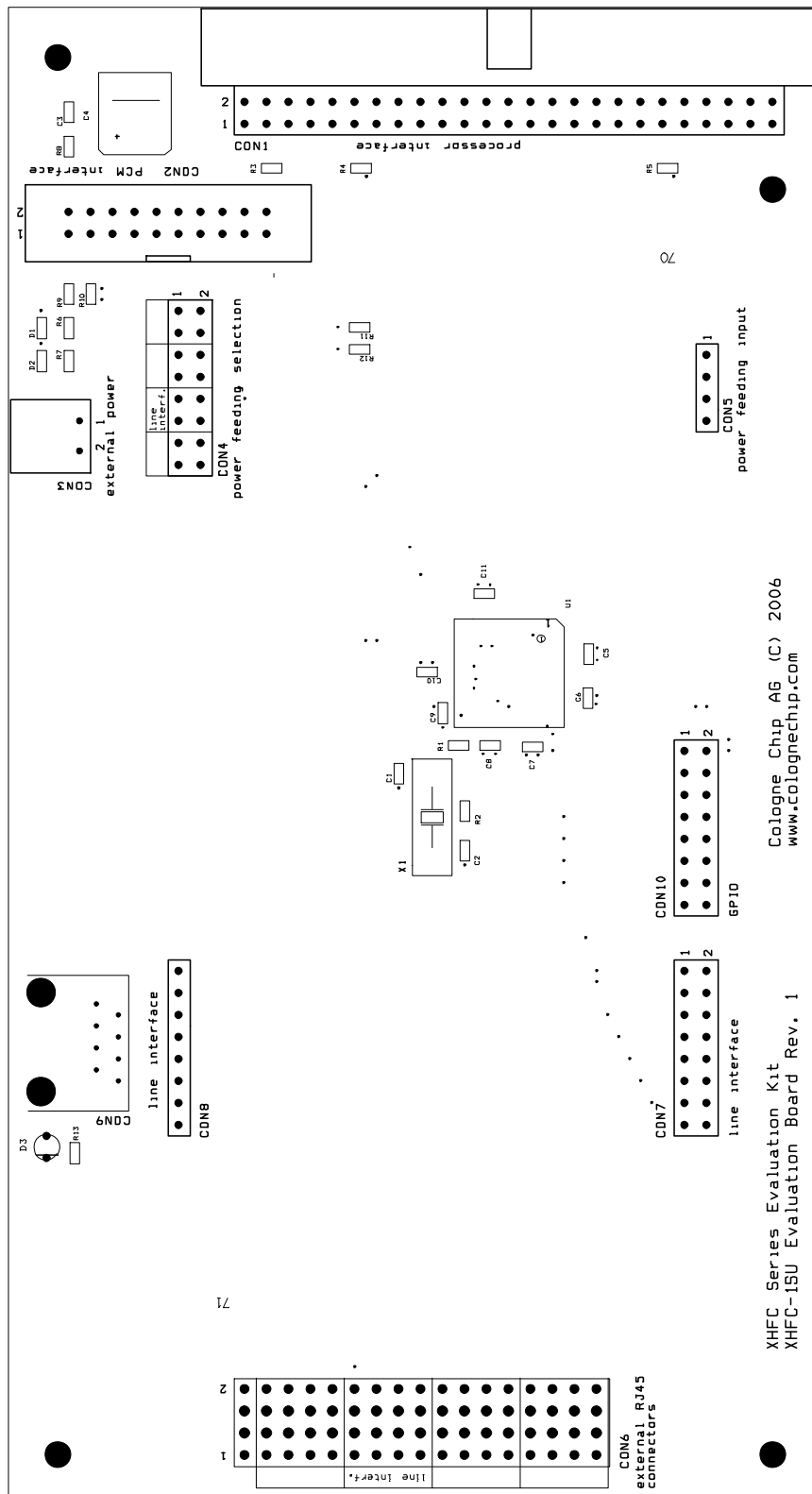


Figure 5: XHFC-1SU Evaluation Board board (top side inscription)

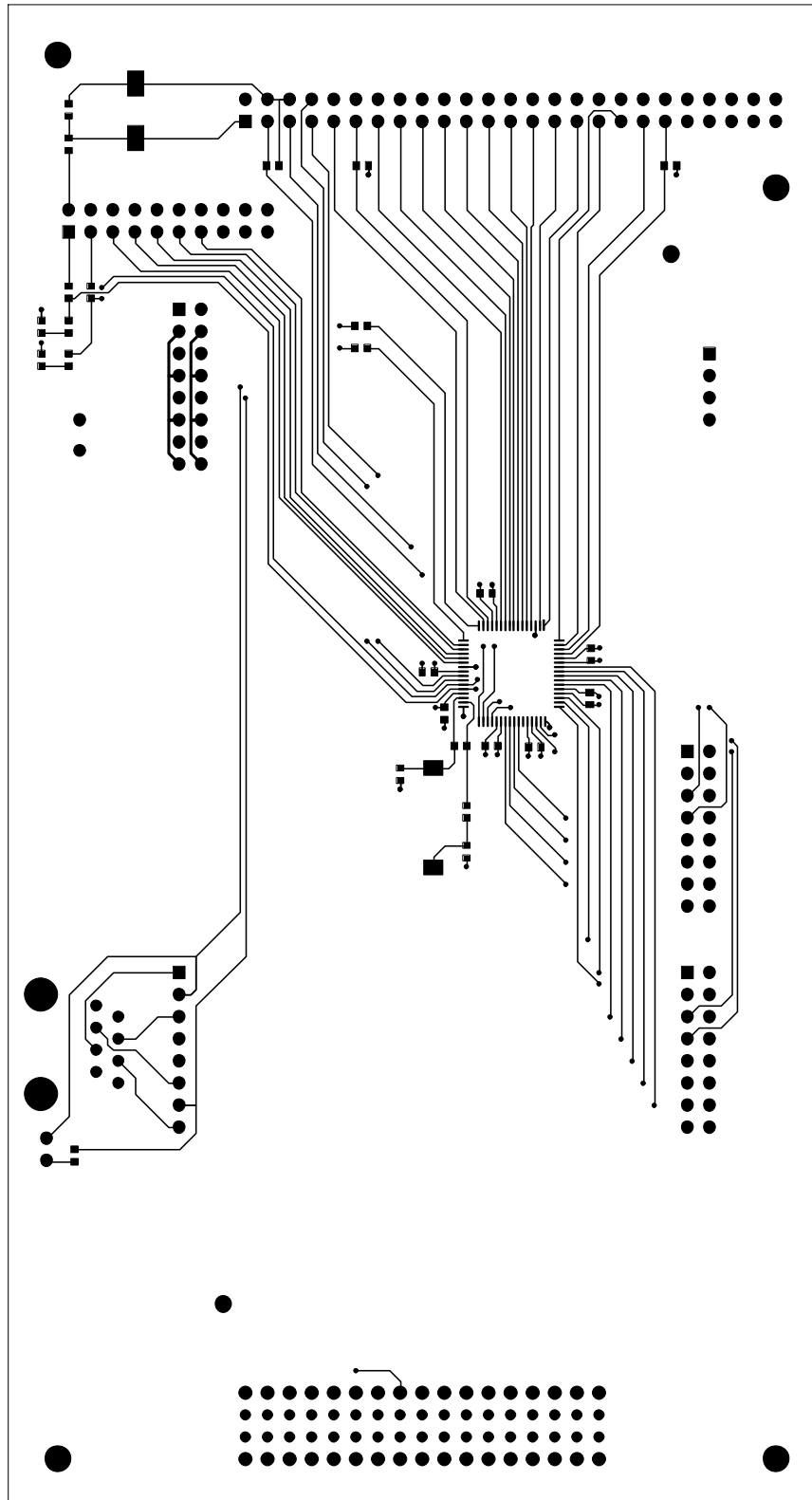


Figure 6: XHFC-1SU Evaluation Board board (top side traces)

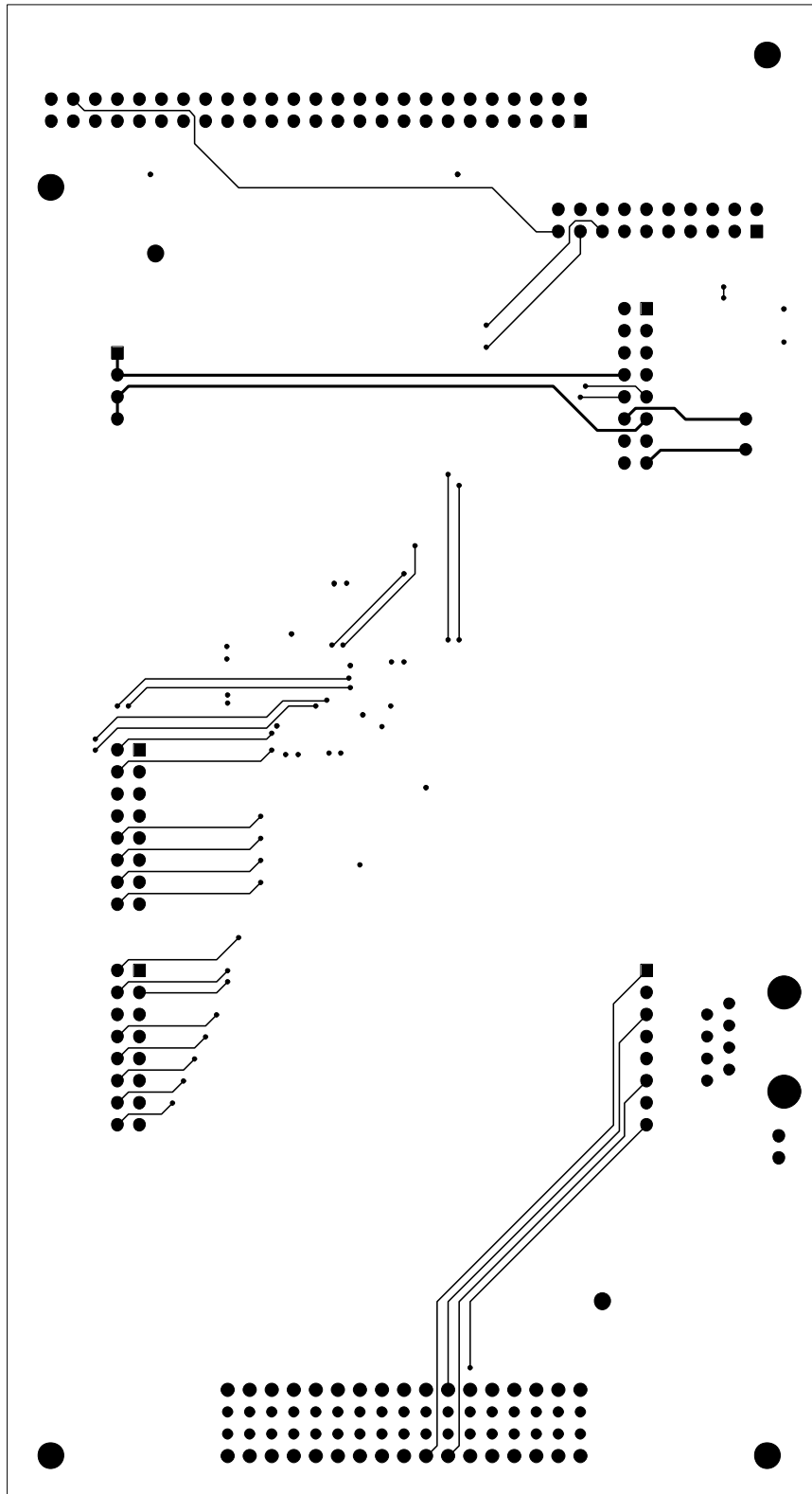


Figure 7: XHFC-1SU Evaluation Board board (bottom side traces)

## References

- [1] Cologne Chip AG. *XHFC-1SU, Extended ISDN HDLC FIFO controller with Universal ISDN Port (data sheet)*, June 2012.
- [2] Cologne Chip AG. *XHFC Series Evaluation Kit. Line Interface Subassembly Rev. 2, S/T Port*, January 2007.
- [3] Cologne Chip AG. *XHFC Series Evaluation Kit. S/T Port Line Interface Subassembly (for NT Mode only) Rev. 2*, January 2007.
- [4] Cologne Chip AG. *XHFC Series Evaluation Kit. S/T Port Line Interface Subassembly with Software Configuration Rev. 1*, January 2007.
- [5] Cologne Chip AG. *XHFC Series Evaluation Kit. Line Interface Subassembly Rev. 2, U<sub>pN</sub> / U<sub>p0</sub> Port*, January 2016.
- [6] Cologne Chip AG. *XHFC Series Evaluation Kit. ST/Up Port Line Interface Subassembly with Coding Plug Rev. 1*, January 2007.
- [7] Cologne Chip AG. *XHFC Series Evaluation Kit. ST /Up Port Line Interface Subassembly with Automatic Detection Rev. 2*, April 2009.

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