

# HFC - E1 Evaluation Board

## Switches and Jumper

November 2003

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<b>List of Switches:</b>	<b>Code</b>	<b>Description</b>
	JP 11	TE / NT (LT) mode switch
	JP 21	Termination of the E1 interface

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<u>List of Jumpers:</u>	<u>Code</u>	<u>Description</u>
	JP 1	3.3 V aux power supply
	JP 2	E1 transmit and receive signals (RJ45 jack side)
	JP 3	Interface mode selection, MODE1 to VDD
	JP 4	Interface mode selection, MODE0 to VDD
	JP 5	E1 transmit and receive signals (chip side)
	JP 6	E1 transmit signal (transformer side)
	JP 7	E1 receive signal (transformer side)
	JP 8	3.3 V measurement and test lead from PCI interface
	JP 9	3.3 V measurement and test lead from PCI interface
	JP 10	EE_SCL/EN to GND, disables EEPROM if connected
	JP 13	SPI connector
	JP 14	Auxiliary port or SRAM interface
	JP 15	GPI[23..16], GPIO[11..8]
	JP 16	GPI[31..24], GPIO[15..12]
	JP 17	PCM port and EEPROM test leads
	JP 18	3.3 V measurement and test lead
	JP 19	GND measurement and test lead
	JP 20	GPI[15..4], GPIO[7..2]

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- JP 8 and JP 9 are hard wired (i.e. connected). If JP 1 is connected, JP 8 and JP 9 must both be disconnected by cutting open the wire! **Otherwise the PCI interface might be damaged!**



For more information or questions please contact Cologne Chip AG at [support@colognechip.com](mailto:support@colognechip.com)