IP/SOC 2006

Session : Mixed Signal IP

FULLY DIGITAL IMPLEMENTED PHASE LOCKED LOOP

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Abstract

One of the most challenging tasks in analog circuit design is to adapt a functional block to ever new CMOS process technology. For digital circuits the number of gates per square mm approx. doubles per chip generation. Integration of analog parts in recent deep submicron technologies is much more difficult and additionally complicated because the usable voltage ranges are decreasing with every new integration step.

This paper shows an approach for a PLL that only uses digital cell libraries. So all integration advantages of pure digital chips are preserved, there is no design effort for a new chip generation and the PLL also can be used in a FPGA.

One of the most astonishing feature is the possibility to check the whole functionality with a pure digital simulator. So without an analog simulator like Spice performance values like frequency and jitter can be checked.

Furthermore the here introduced PLL has the ability to relock in a very short time after the oscillator is enabled after a power down period. This is a key feature for some battery driven applications where the lock time of the PLL is a significant share of the operation time itself.

1. Motivation

Phase Locked Loops (PLLs) are a widely needed and used circuitry in today's semiconductor chips [1]. They are used for 3 different tasks:

a) generation of high speed on chip clocks by frequency multiplication
b) deskew of clocks to reduce clock skew
c) jitter attenuation

A PLL is characterized by the frequency range, jitter, jitter attenuation and lock time. PLLs of type a) are only used for generation of high speed stable clocks and are normally fed by quartz controlled oscillators so that there is no need for a jitter attenuation.

Traditional PLLs are composed of a voltage controlled oscillator (VCO) as clock source, a phase and/or frequency comparator, a loop filter and a frequency devider (Fig. 1). Usually the VCO clock is divided by an integer divider and then compared to a reference clock which is input to the PLL. The compare result as phase and/or frequency difference is converted into a voltage which controls the VCO. This converter normally is a simple low pass filter. It is called "loop filter".
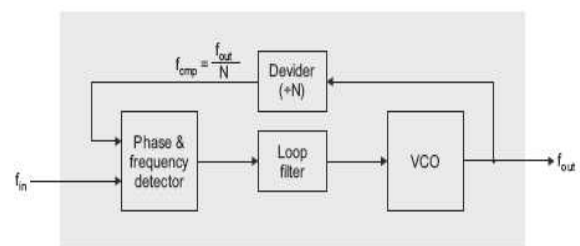

Fig. 1: Traditional PLL

The jitter of the VCO and so the jitter of the output frequency is due to different mechanisms. These are random jitter, jitter introduced by noise on the voltage control input of the VCO, adjust voltage pulses coming through the loop filter and supply voltage noise.

The lock time of a PLL is defined as the time that elapses from initial or reset condition till the phase locked generation of the output frequency. It is

mainly influenced by the phase comparator and the loop filter.

Unfortunately PLLs are up to now mixed-mode circuitries that must combine analog parts as loop filter and VCO with digital parts as the frequency divider.

So at least the analog circuitry must be adapted to every new CMOS process technology. For digital circuits the number of gates per square mm approximately doubles per chip generation. Integration of analog parts in recent deep submicron technologies is much more difficult and additionally complicated because the usable voltage ranges are decreasing with every new integration step. So deep submicron technologies use core voltages in the range of 1V only. Also some area is needed to realize accurate parameters.

Especially difficult is to reduce the size of the loop filter, because a capacitor of significant size is needed.

If it would be possible to realize a PLL as "pure" digital circuit no effort would be needed to scale the device for ever new CMOS process technology and furthermore the full integration advantage of a digital circuit would be feasible. Additionally no special silicon process and test technology known as "mixed-mode" would be needed.

2. Overview

The goal of the new DIGICC^{TM} PLL technology is that all components of a high performance PLL are really fully digital. There is no need for external components as loop capacitors, special I/Os or special GND or VDD pins. Even there is no need for a special location for the PLL on the die.
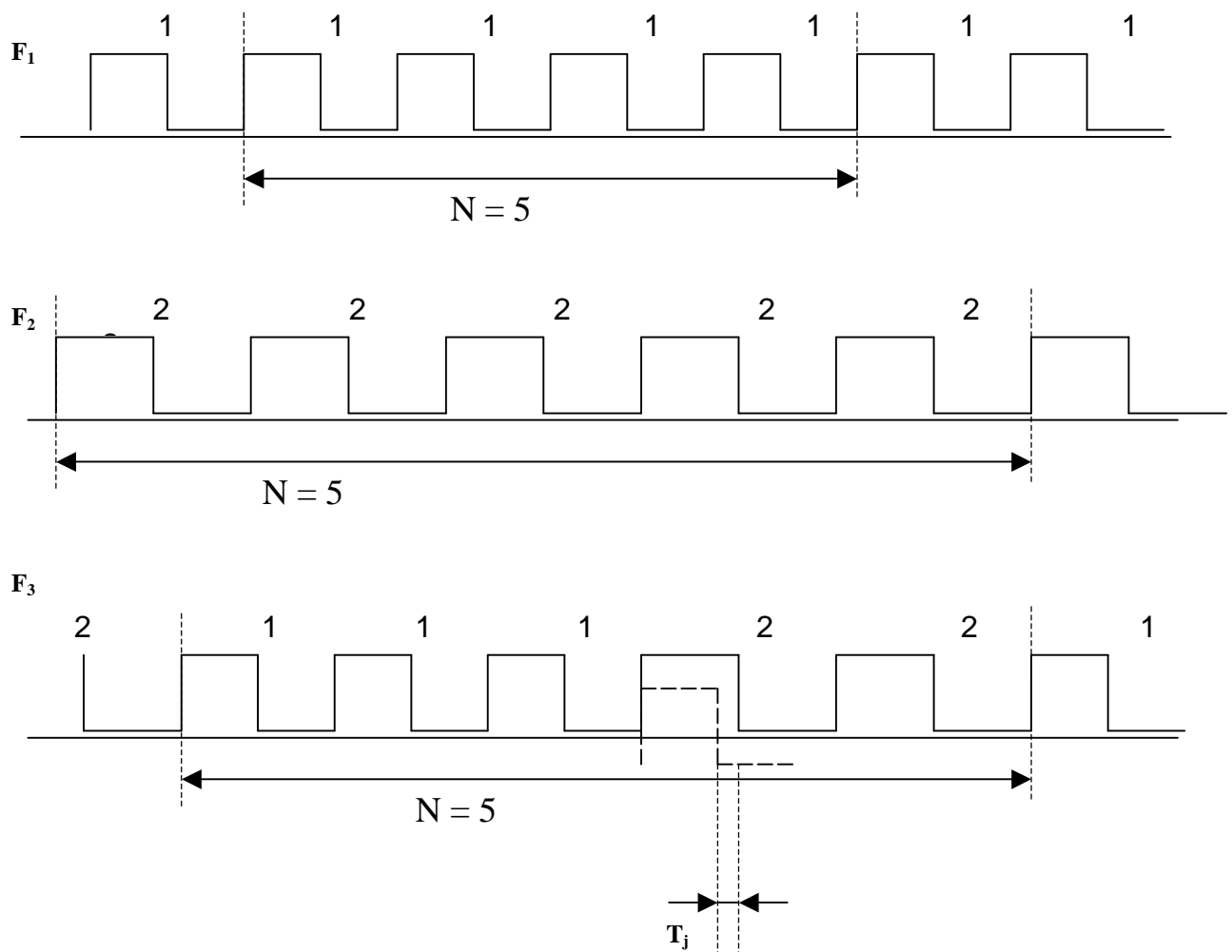

Fig. 2: Frequency composition from pulses of two different frequencies F_1 and F_2

3. Realization

The DIGICC^{TM} PLL approach changes the method of frequency generation.

Any output frequency can be generated by ongoing switching between 2 frequencies where the frequency F_1 is higher and the frequency F_2 is lower than the frequency F_3 which is to be generated (see Fig. 2). The maximum clock-to-clock jitter is the difference of the period length of F_1 and F_2. It is shown in Fig. 2 as Tj. So if the frequency difference between the two frequencies is very low the jitter is also very low.

3.1. Digital controlled oscillator

The two frequencies can be generated by a digital controlled oscillator (DCO). This circuitry uses gate delays to control the frequency of the oscillator. By multiplexers or switches the frequency can be changed. Also slight adjustments can be made by changing the load of a gate. So it is easy to design a DCO which has a big range for the output frequency and only very low frequency changes for one step.

The realization is fully digital because only gate delays are used as frequency controlling elements.

Because there is no controlling voltage as it is the case for a VCO there is no noise introduced jitter for the so realized DCO. The main jitter source is the supply voltage because all gate delays in a digital circuitry are influenced by the supply voltage. Even if there is no special separated supply voltage for the PLL used the supply voltage induced jitter is in the 1%..5% range.
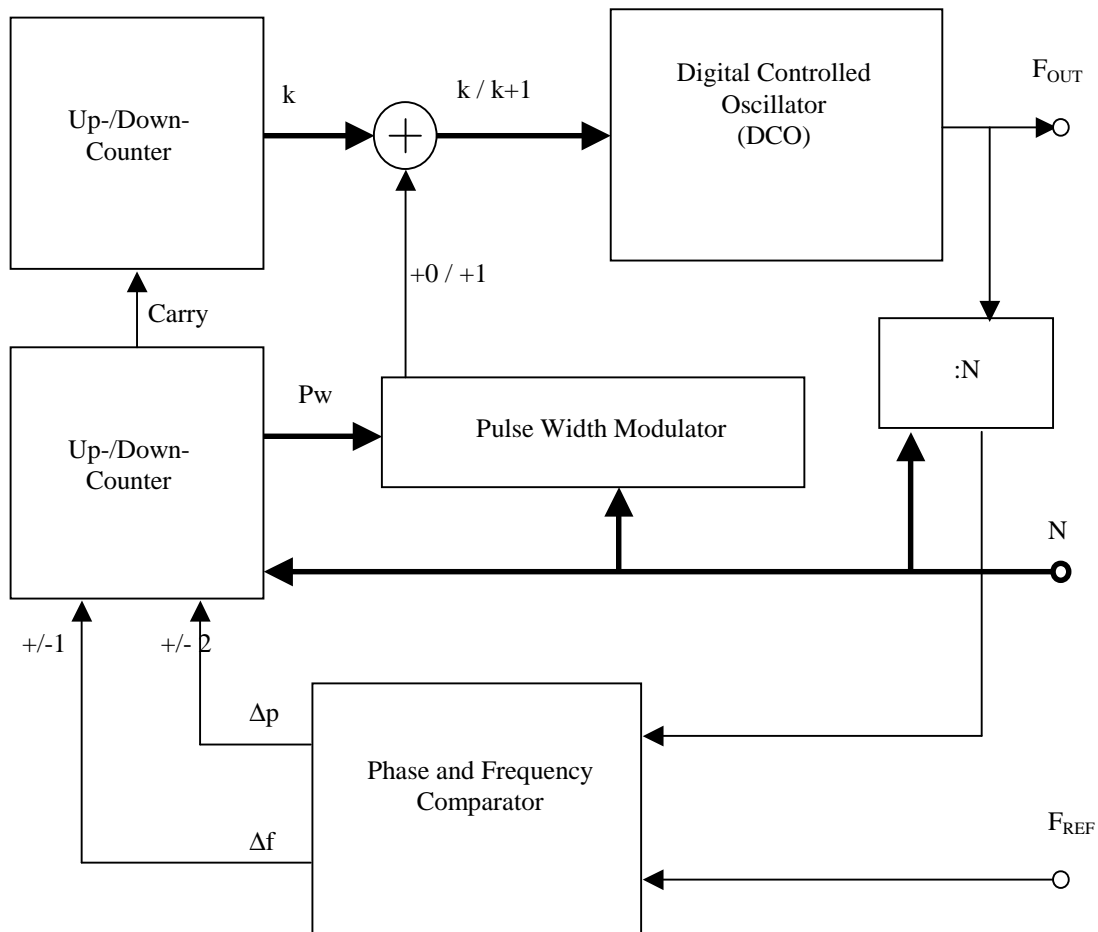

Fig. 3: Sample Schematic of a DIGICC^{TM} type PLL for frequency multiplication by a factor N

3.2. Pulse width modulated switching

The switching between the two frequencies can be optimized so that the over all jitter is minimized. This is done by switching just when the phase of the output frequency overtake or undertake the ideal phase of the output frequency. This is identical to a switching in the shortest possible distances. This way of switching simply can be generated by a pulse width modulator (PWM). This device generates a programmable number of '1's in a period of n clocks and furthermore distributes the '1's in a way that the mean gap between two '1's is minimized. So with a PWM all frequencies between F_1 and F_2 can be generated depending of the range of the PLL. Fortunately the introduced clock-to-clock jitter Tj is always the same and is only due to the difference between the two clock frequencies.

3.3. Phase and Frequency comparators

Because in the DIGICC^{TM} type PLL no analog components are implemented it is not possible to measure the phase difference between the reference frequency and the divided oscillator frequency. So the phase transition is detected and as result of this the frequency of the DCO is slightly adjusted in a way that there must be a phase transition in the opposite direction. So there is an oscillation around the exact output frequency which should be generated. Furthermore the frequency of the oscillator is adjusted if there is a better center frequency for this oscillation.

Both adjustment pathes are shown in Fig. 3.

3.3. Jitter Scaling

For many PLL application it is even not the best solution to reduce the output jitter to the smallest value possible. This is due to the fact that problems known as EMI are increased if the power spectrum is just concentrated at one frequency. So e.g. for the clocking of processor systems a defined increase in jitter can reduce EMI problems. Jitter can easily increased in DIGICC^{TM} type PLLs by increasing the smallest frequency increment of the DCO.

3.4. Lock Time

Because the DIGICC^{TM} type PLL don't include any analog loop filter the achievable lock times are lower than these for traditional PLLs. Furthermore the PLL can be "frozen" for an arbitrary time interval and is locked again in a very short time because the actual operation status is digitally stored in the up/down-counter of the PLL. No discharge of a capacitor or similar will influence the lock again time after new start of oscillation.

4. Implementation as high speed PLL in a FPGA

The herein described DGICC^{TM} PLL technology even was implemented into different VIRTEX^{TM} type FPGAs from XILINX. Due to the implementation in CLBs instead of real gates the performance of the PLL is decreased.

4.1. Measurement results

For the FPGA implementation the following values were measured.

PLL output frequency:	125 MHz
Reference frequency:	5 MHz
Typical Jitter:	+/-270 ps
	(Sigma 150 ps)
Worst Case Jitter:	+/- 490 ps
	(Sigma 190 ps)
Jitter from Supply Voltage:	120 ps / 100 mV
Lock time (maximum):	2000 Clocks
	(< 400 us)

5. Performance analysis

An other valuable benefit of the DIGICC^{TM} type PLL is the ability to check the performance and center frequency using normal digital simulation technology. Because the circuitry is composed of normal digital gates only it can be simulated by high speed event driven digital simulators. Even jitter attenuation and the reaction on jitter at the reference input can be simulated easily.
In contrast to mixed mode PLL IP blocks the user only can rely on the specification which is provided by the vendor or designer. Only much more time consuming analog simulation can evaluate mixed mode type PLL cores.

6. Conclusion

DIGICC^{TM} is a highly sophisticated new approach for a wide range of PLLs. It realizes mixed mode requirements with pure digital IP cores.

No external components as additional power Pads/Pins, loop capacitors or similar is needed. So a seamless integration in every new chip process technology is achieved and the scaling factor of a new digital chip generation can be fully exploited.

Literature

[1] Fahim, Amr M., "Clock Generators for SOC Processors / Circuits and Architectures", *Springer Science+Business Media, Inc.,* e-ISBN 1-4020-8080, 2005