Cologne Chip

C3 - CODEC - G712 - 4

Quad Voice CODEC compliant to ITU G.712

Implemented in DIGICC™ Technology

C3 IP

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1 DIGICC™ technology

Background

Being successful in ASIC design for over ten years, the experience of Cologne Chip's R&D team in digital engineering has led to an in-depth know-how especially in the field of telecommunication interfaces. Millions of sold microchips underline the company's expertise in ASIC and FPGA design. This core competence of Cologne Chip becomes now IP core competence: Cologne Chip introduces several ASIC IPs to the market under the brand name C3IP.

Design approach

The most innovative products of these Cologne Chip IP cores for CMOS devices are based on the entirely new DIGICC™ technology. DIGICC™ increases the range of applications which can be handled by pure digital circuitries.

Up to now PLLs and furthermore analog-to-digital converters (ADC) and digital-to-analog converters (DAC) need a big portion of analog circuitry on the chip. Traditional PLLs need a voltage controlled oscilator (VCO) and loop filter. ADCs – even realized as delta sigma converters – traditionally need some switched capacitor integrators and other analog circuitries. DIGICC™-based cores offer full digital macros for these analog functions. This sounds "impossible" even for the experienced hardware engineer – but it works!

So the biggest benefit of the introduced IP cores is the scalability over a wide range of chip process technologies without requiring design efforts for each new technology. Furthermore, the DIGICC™ IP cores require less silicon space then comparable analog counterparts.

The IP cores can also be integrated in some FPGA technologies at small trade-offs.

All cores are evaluated in silicon and are even used in FPGA technology. They can easily be implemented in different digital CMOS circuits in a broad range of ASIC applications.

The DIGICC™ IP cores are protected by patents and other commercial rights.

Products

Cologne Chip introduces DIGICC™ cores for two fields of applications: C3-PLL and C3-CODEC. For both product families the analog functionality is realized with a completely digital core circuitry using standard cell libraries.

Please ask our support team for more information on these IP cores.

2 C3-CODEC-G712-4 overview

Standard CODECs need always some analog parts for the integration of analog-to-digital and digital-to-analog conversion. Cologne Chip has come up with a fully digital approach now. The C3-CODEC-G712-4 core implements four CODECs for a broad range of telecommunication applications.

All analog characteristics of a CODEC are moved into a few external resistors and capacitors. These external components are connected to three digital I/O buffers. This way of implementing analog features to fully digital CMOS circuitries is in accordance with the DIGICC™ technology of Cologne Chip. There are sophisticated digital machines in the feedback logic to minimize the external component cost.

The C3-CODEC-G712-4 is based on the DIGICC™ technology of Cologne Chip, which makes it possible to be easily implemented in all kinds of digital CMOS circuits as a fully digital circuit. A patent is pending for this new Cologne Chip CODEC technology.

2.1 Technical features

- 4 voice CODECs implemented within one core
- Fully digital core
- Internal data format configurable to either 16 bit linear or 8 bit a-law / μ-law according to ITU-T recommendation G.711 [2]
- Performance of the signal path according to ITU-T recommendation G.712 [1]
- Implementable in any CMOS process technology
- Implementable also into FPGA with external digital buffers
- Only 3 digital I/O pins and one power supply pin required for every CODEC
- Only few resistors and capacitors required as external components
- The signal-to-total distortion complies ITU-T recommendation G.712 [1]
- Suppression of 50 Hz and 60 Hz in the ADC is better than 45 dB
- Gain for the transmit path (ADC) and the receive path (DAC) for each CODEC separately progammable
- Power reduction to nearly zero in stand-by mode
- 8 k sample/s or 16 k sample/s configurable
- 24.576 MHz clock frequency (other frequencies on request, see requirements in section 4.4)
- Chip area:

  C3-CODEC-G712-4: about 60 k logic gates, depends on technology library and test methodology

  RAM: 7.68 kbit RAM, divided into 4 synchronous single port RAM blocks (data: 128 × 32, 64 × 32, parameter: 64 × 16, 32 × 16)
- Core version with only three, two or one CODEC available (reducing by one CODEC decreases the core by about 6 k gates and 1.92 kbit RAM)

2.2 Application fields

The C3-CODEC-G712-4 is an IP core which is interesting for several application fields:

- Voice CODEC for PABX
- Voice CODEC for telephones
- Voice CODEC for line cards
- Voice CODEC for VoIP

3 C3-CODEC-G712-4 pinout

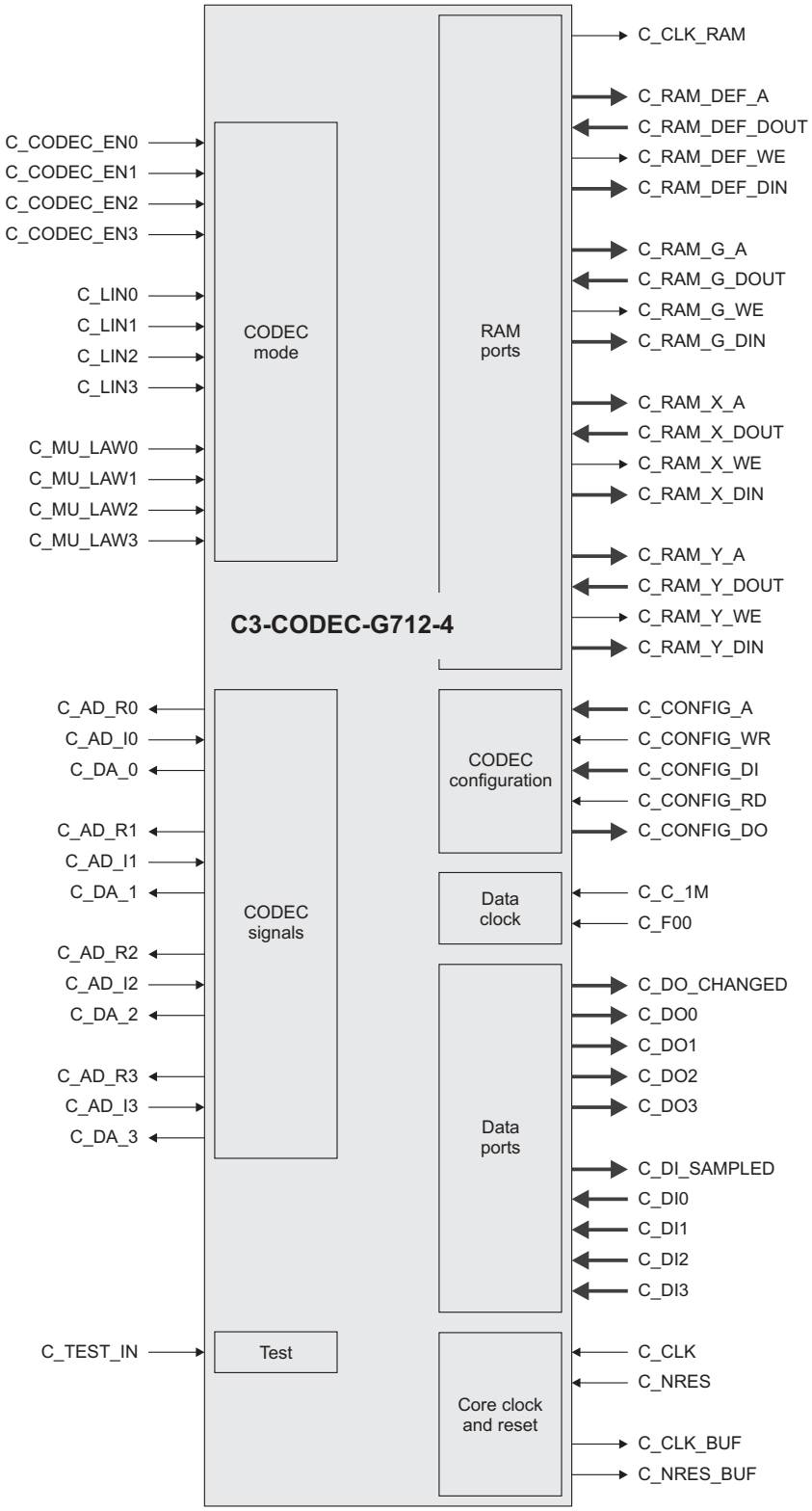

Figure 1: *C3-CODEC-G712-4 pinout*

Table 1: *Pin description of C3-CODEC-G712-4 (Figure 1)*

Name	I/O	Description
C_CODEC_EN0 . . C_CODEC_EN3	I	CODEC enable '0' = C_AD_Rx and C_DAx output pins to the analog front-end remain static; the clock of the core stops if all enable signals are low (power consumption is nearly zero) '1' = CODEC x is enabled
C_LIN0 . . C_LIN3	I	'0' = Logarithmic data format according C_MU_LAWx is selected, data bits [7:0] are used '1' = 16 bit linear data format is selected, data bits [15:0] are used
C_MU_LAW0 . . C_MU_LAW3	I	Configuration of the encoding law if C_LINx = '0' '0' = a-law encoding according G.711 '1' = μ-law encoding according G.711
C_AD_R0..C_AD_R3	O	Feedback output to the analog front-end of the ADC
C_AD_I0 . . C_AD_I3	I	Input from the analog front-end of the ADC
C_DA_0 . . C_DA_3	O	Output to the analog front-end of the DAC
C_TEST_IN	I	Test input
C_CLK_RAM	O	Clock for the synchronous RAMs, only rising edge used
C_RAM_DEF_A	O[6:0]	Address lines of filters D, E and F
C_RAM_DEF_DOUT	I[31:0]	Data lines from RAM of filters D, E and F
C_RAM_DEF_WE	O	Write enable of filters D, E and F
C_RAM_DEF_DIN	O[31:0]	Data lines to RAM of filters D, E and F
C_RAM_G_A	O[5:0]	Address lines of filter G
C_RAM_G_DOUT	I[31:0]	Data lines from RAM of filter G
C_RAM_G_WE	O	Write enable of filter G
C_RAM_G_DIN	O[31:0]	Data lines to RAM of filter G
C_RAM_X_A	O[5:0]	Address lines of filter coefficients X
C_RAM_X_DOUT	I[15:0]	Data lines from RAM of filter coefficients X
C_RAM_X_WE	O	Write enable of filter coefficients X
C_RAM_X_DIN	O[15:0]	Data lines to RAM of filter coefficients X
C_RAM_Y_A	O[4:0]	Address lines of filter coefficients Y
C_RAM_Y_DOUT	I[15:0]	Data lines from RAM of filter coefficients Y
C_RAM_Y_WE	O	Write enable of filter coefficients Y
C_RAM_Y_DIN	O[15:0]	Data lines to RAM of filter coefficients Y

(continued on next page)

Table 1: *Pin description of C3-CODEC-G712-4 (Figure 1)*

(continued from previous page)

Name	I/O	Description
C_CONFIG_A	I[11:0]	Address of the configuration port
C_CONFIG_WR	I	Write pulse
C_CONFIG_DI	I[15:0]	Data input lines for write operation
C_CONFIG_RD	I	Read pulse
C_CONFIG_DO	O[15:0]	Data output lines for read operation
C_C_1M	I	1024 kHz clock pulse
C_F00	I	8 kHz frame synchronization pulse
C_DO_CHANGED	O[3:0]	Handshake of the data output pathes to indicated new data; C_DO_CHANGED [0] is assigned to C_DO0, C_DO_CHANGED [1] is assigned to C_DO1, etc.
C_DO0 . . C_DO3	O[15:0]	Data output of the transmit path (ADC); data format is either 16 bit linear ([15:0] in 2th complement) or 8 bit a-law / μ-law at [7:0]; MSB is bit 15 or bit 7, LSB is bit 0
C_DI_SAMPLED	O[3:0]	Handshake of the data input pathes to indicate when data is accepted; C_DI_SAMPLED [0] is assigned to C_DI0, C_DI_SAMPLED [1] is assigned to C_DI1, etc.
C_DI0 . . C_DI3	I[15:0]	Data input of the receive path (DAC); same data format as C_DOx
C_CLK	I	24.576 MHz core clock (23.900 MHz . . 25.100 MHz maximum range, see requirements in section 4.4); the rising edge is mainly used; C_CLK has its own buffer inside the core
C_NRES	I	Asynchronous reset; C_NRES has its own buffer inside the core '0' = reset '1' = normal operation
C_CLK_BUF	O	C_CLK output
C_NRES_BUF	O	C_NRES output

4 Functional blocks

The C3-CODEC-G712-4 core implements four CODECs as shown in the block diagram in Figure 2.

Every CODEC has its own enable signal C_CODEC_EN0 . . C_CODEC_EN3. Two additional pins per CODEC are used for encoding / decoding features.

4.1 Analog-to-digital converter

Every CODEC uses two pins for the analog-to-digital conversion (ADC). Both the input signal and the feedback signal can be inverted to fulfill any application needs.

The transmit path (ADC) consists of

- the feedback logic to realize the ADC,
- several filter stages of low-pass filter to reduce the sample rate from 24.576 MHz to 64 kHz and a two-stage band-pass filter from 64 kHz to 8 kHz which fulfills the requirements of ITU G.712 [1], especially the attenuation versus frequency distortion,
- programmable gain factor,
- the encoding stage to support the formats linear or a-law or μ-law
- the digital output register of the transmit path, changing their values with C_DO_CHANGED.

4.2 Digital-to-analog converter

Every CODEC uses one pin for the digital-to-analog conversion (DAC). The output signal can be inverted.

The receive path (DAC) consists of

- the digital input register which take over the data with C_DI_SAMPLED
- the decoding stage to support the formats linear or a-law or μ-law
- programmable gain factor,
- the interpolation filter to raise the sample rate from 8 kHz to 64 kHz,
- the errror feedback modulator which converts the parallel data stream to a noise shaped 1-bit stream to drive the external RC analog part.

4.3 Digital filters

The main part of the core area is used for the digital filters in the transmit and the receive path according to the ITU-T recommendation G.712 [1].

They implement band-pass filtering in the transmit path from the ADC to the internal digial interface and low-pass filtering in the receive path to the DAC. In the ADC the high sampled data from the delta sigma like front-end are decimated to the signal band from 300 Hz to 3400 Hz (8 k sample/s). In the DAC the input data is interpolated to a higher internal sample frequency and then converted with an error feedback modulator. Both pathes use several filter stages with IIR structure to fulfill the

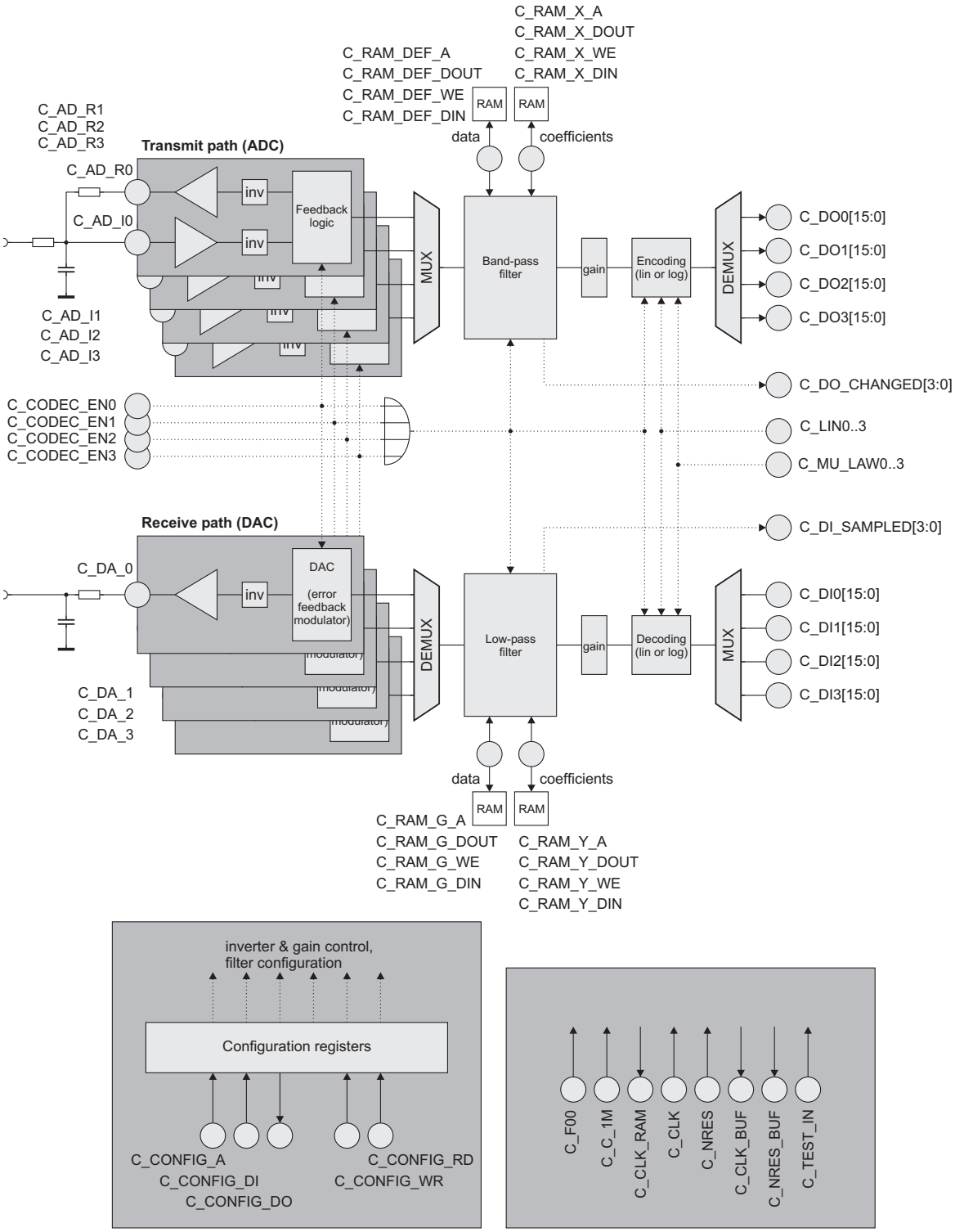

Figure 2: *C3-CODEC-G712-4 block diagram*

recommendations ITU G.712 [1]. The data and coefficients of the filters are stored in four external RAM blocks.

The gain of the transmit path (ADC) and the receive path (DAC) and some configuration bits can be changed via the configuration interface. This interface supports read and write operations. It is also used to test the RAM blocks.

4.4 Core clocks

System clock input

The typical C3-CODEC-G712-4 system clock is C_CLK = 24.576 MHz. However, C3-CODEC-G712-4 can operate within the range 23.900 MHz ≤ C_CLK ≤ 25.100 MHz, but 24.576 MHz is recommended because this frequency can easily be used to generate the required data synchronization clocks.

The system clock C_CLK must be stable during operation. Valid duty cycle of is 40:60 . . 60:40.

C_CLK is internally buffered to C_CLK_INTERNAL and the whole core operates on C_CLK_INTERNAL.

Data synchronization clock inputs

The data operation is based on the 8 kHz frame synchronization signal on the clock input pin C_F00. An additional data synchronization clock C_C_1M = 1024 kHz is also required.

C_F00 and C_C_1M can have an arbitrary phase but must have a constant phase to each other. There must be exactly 128 C_C_1M pulses between two successive C_F00 pulses. C_F00 and C_C_1M are sampled synchronous to the rising edge of C_CLK_INTERNAL. If possible, they should be generated synchronous to the falling edge of C_CLK.

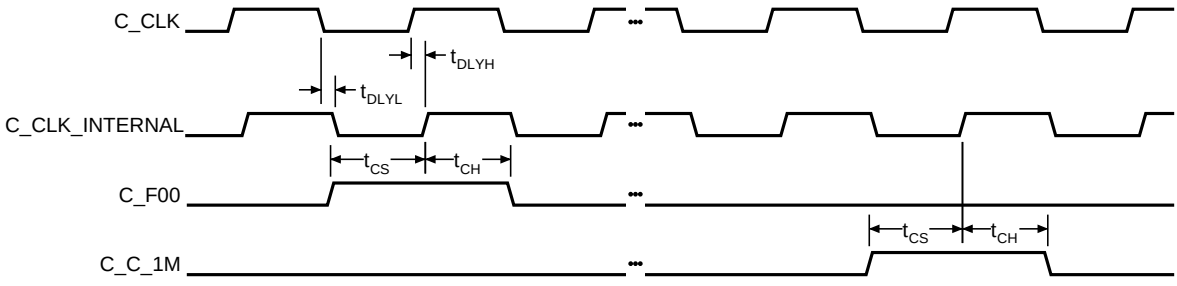

Figure 3: *Data synchronization clocks*

The data synchronization clocks are shown in Figure 3. It is recommended to generate the high time of C_C_1M and C_F00 for one C_CLK cycle. However, both signals can have an arbitrary, individual high time. The first sample which is high will be used in the core.

Please note, that C_C_1M and C_F00 frequencies do not depend on the operating mode, especially 8 k sample/s or 16 k sample/s data rate.

Table 2: *Symbols of data synchronization clocks in Figure 3*

Symbol	min / ns	max / ns	Characteristic
t_{DLYL}	0	3	Clock input to internal clock delay (falling edge)
t_{DLYH}	0	3	Clock input to internal clock delay (rising edge)
t_{CS}	10		Synchronization clock setup time
t_{CH}	5		Synchronization clock hold time

Please note !

When C_CLK = 24.576 MHz is used, C_C_1M and C_F00 can be generated by dividers. A different C_CLK frequency can be used. The permissible frequency range is 23.900 MHz ≤ C_CLK ≤ 25.100 MHz

But C_F00 must be 8 kHz and C_C_1M must have exact 128 pulses between every two pulses of C_F00.

The small difference between C_C_1M pulses and 24 cycles of C_CLK is allowed. The C3-CODEC-G712-4 core requires 23 cycles between successive C_C_1M pulses. So a variation of the frequence ratio between C_C_1M and C_CLK around the nominal value 24 is possible and leads to a situation that C_C_1M intervals mostly match 24 cycles and sometimes 23 or 25 cycles.

4.5 Data interface

The data interface of the C3-CODEC-G712-4 consists of four 16 bit data output busses C_DO0 . . C_DO3 and four 16 bit data input busses C_DI0 . . C_DI3. Either 16 bit linear or 8 bit logarithmic data format is available. If 8 bit format is selected only bits [7:0] are used. The encoding for the 8 bit format is configurable to a-law or μ-law as described in the recommendation ITU G.711 [2].

Handshake signal output

Two handshake signals are generated for the data interface. They are used to control the data flow between C3-CODEC-G712-4 and an external data source and destination.

- C_DO_CHANGED indicates when new data is available at the data output port C_DO[15:0].
- C_DI_SAMPLED indicates when the data at input port C_DI[15:0] has been sampled.

C_DO_CHANGED and C_DI_SAMPLED are generated from C_C_1M and C_F00. They both have a frequency of either 8 kHz (8 k sample/s) or 16 kHz (16 k sample/s).

Timing characteristics

Figures 4 and 5 show the timing characteristics of the data interface.

Output data changes always on the rising edge of C_CLK_INTERNAL. It should be read with the falling edge of C_CLK during C_DO_CHANGED is high.

Input data is sampled on the rising edge of C_CLK_INTERNAL. It should be changed with the falling edge of C_CLK. C_DO_SAMPLED indicates that the data was sampled.

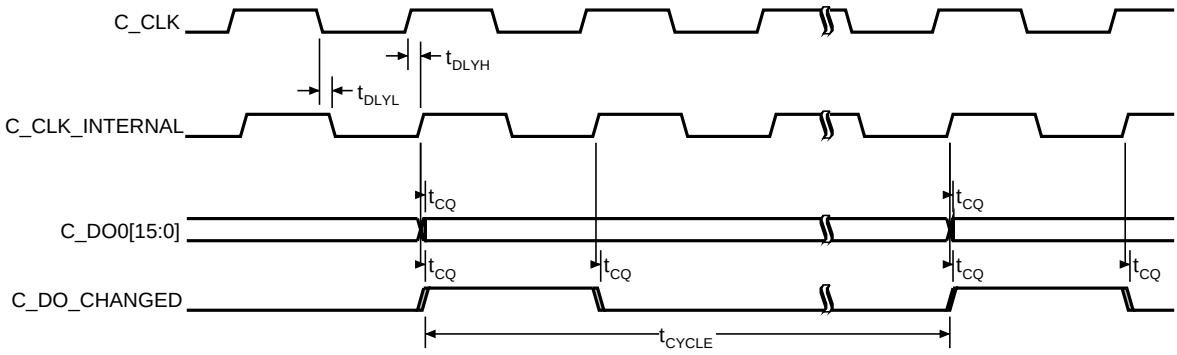

Figure 4: *Data output interface signals*

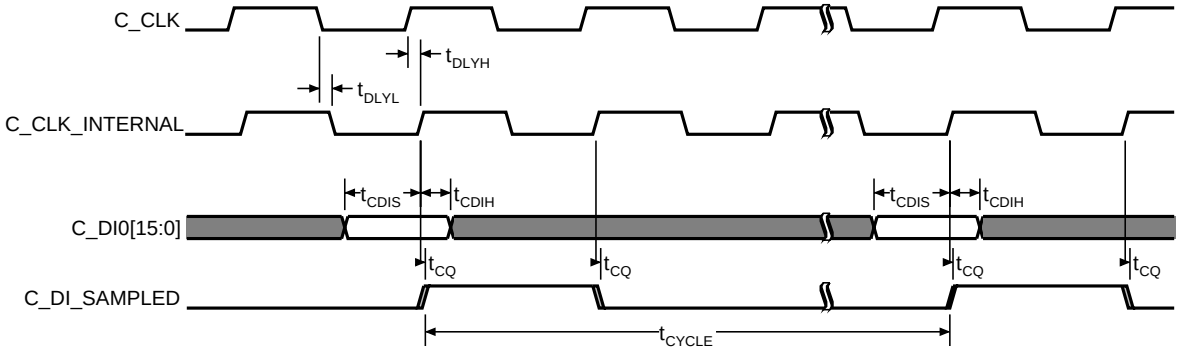

Figure 5: *Data input interface signals*

Table 3: *Symbols of data output and data input interfaces in Figures 4 and 5*

Symbol	min / ns	typ / ns	max / ns	Characteristic
t_{DLYL}	0		3	Clock input to internal clock delay (falling edge)
t_{DLYH}	0		3	Clock input to internal clock delay (rising edge)
t_{CQ}	0		1	Internal clock to signal stable delay
t_{CDIS}	10			Data setup time
t_{CDIH}	5			Data hold time
t_{CYCLE}		125000		Cycle time in 8k-sample mode
		62500		Cycle time in 16k-sample mode

4.6 RAM interfaces

Four RAM interfaces are implemented to store filter coefficients and data. Single ported, synchronous RAM is required for C3-CODEC-G712-4. The RAM should work on rising edges of C_CLK_RAM.

Different RAM sizes are used:

- C_RAM_DEF : 128 × 32 bit (512 bytes)
- C_RAM_G : 64 × 32 bit (256 bytes)
- C_RAM_X : 64 × 16 bit (128 bytes)
- C_RAM_Y : 32 × 16 bit (64 bytes)

Figure 6 shows the timing characteristics of the RAM interface exemplarily for C_RAM_DEF. All RAM interfaces have the same characteristics.

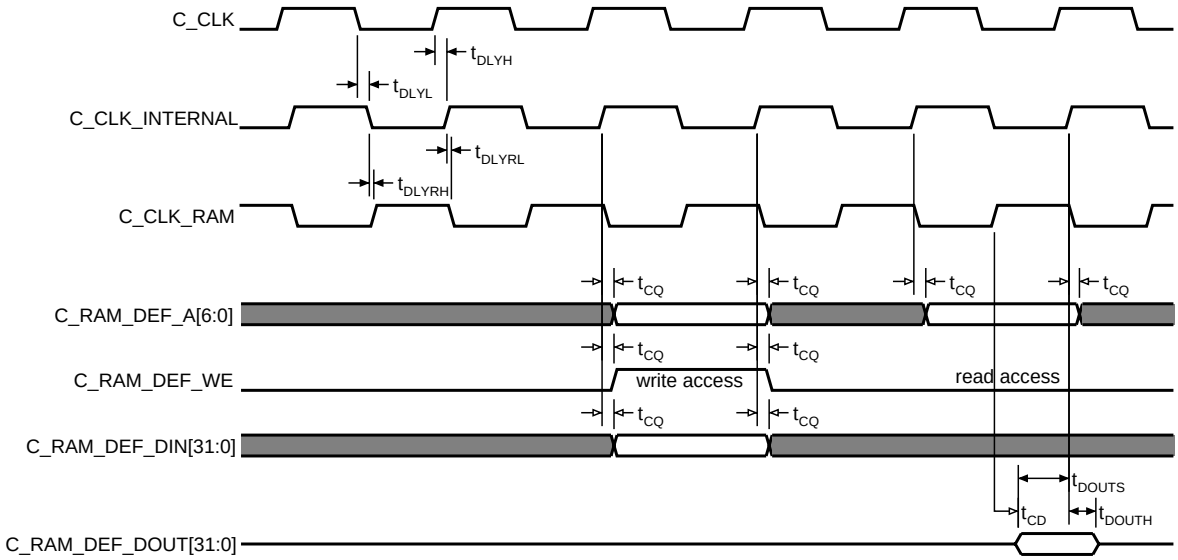

Figure 6: *RAM interface, exemplarily shown for C_RAM_DEF*

Table 4: *Symbols of RAM interface in Figure 6*

Symbol	min / ns	max / ns	Characteristic
t_{DLYL}	0	3	Clock input to internal clock delay
t_{DLYH}	0	3	Clock input to internal clock delay
t_{DLYRH}	0	1	Internal clock to RAM clock delay
t_{DLYRL}	0	1	Internal clock to RAM clock delay
t_{CQ}	0	1	Internal clock to signal stable delay
t_{DOUTS}	10		Data output setup time
t_{DOUTH}	5		Data output hold time
t_{CD}			Clock to data valid delay

5 Internal configuration registers and RAM addresses

5.1 Overview

The configuration port has a data width of 16 bit. Data can be read from the port C_CONFIG_DO[15:0]. Write accesses use the port C_CONFIG_DI[15:0].

All transactions are addressed with the 12 bit address C_CONFIG_A[11:0]. The address structure is shown in Table 5.

Table 5: *Address structure of C_CONFIG_A [11:0]*

Address bits	Purpose	'0' meaning	'1' meaning
[11:10]	CODEC number 0 . . 3		
[9]	Test mode	Normal register access	Test mode (should be tied to '0')
[8]	Path selection	Transmit path (ADC)	Receive path (DAC)
[7]	Area selection	Register area	RAM area
[6]	Register domain, in RAM area only	Data	Coefficients
[5:0]	Specific register selection		

Tables 6 and 7 give a description of the C3-CODEC-G712-4 registers. All registers can be read and written. Please note that all register accesses must specify the CODEC number 0 . . 3 in the address bits C_CONFIG_A[11:10].

A read access to the register IP_ID at address 0x100 returns a 16 bit customer specific IP identifier. This register is read only. [1]

[1] Please note, that register IP_ID is listed neither in Table 6 nor in Table 7.

5.2 ADC registers

Table 6: *Registers for the transmit path (ADC), address must be completed with the CODEC number at C_CONFIG_A[11:10] and C_CONFIG_A[9:8] =* '00'

Name	Area	Address [7:0]	Bits	Reset value	Description
ADC_GAIN	register	0x00	[15:0]	0x1000	ADC gain factor
ADC_CFG	register	0x01			ADC front-end inverter and sample mode
			[0]	0	C_AD_l inverter
			[1]	0	C_AD_R inverter
			[2]	0	Signal-to-filter inverter
			[3]	0	'0' = 8 k sample/s , '1' = 16 k sample/s
			[15:4]	0x000	Not used, must be 0x000
ADC_HYST	register	0x02	[3:0]	8	Hysterese for ADC output data (optional, must be 8)
			[15:4]	0x000	Not used, must be 0x000
ADC_SYNC_POS	register	0x03			This register is valid for every CODEC, i.e. any value of address [11:10] accesses the same register
			[3:0]	0	C_AD_R rising edge to C_DA rising edge phase synchronization (optional, must be 0)
			[15:4]	0x000	Not used, must be 0x000
ADC_FB_TYPE	register	0x04	[1:0]	0	ADC feedback type (optional, must be 0)
			[15:2]	0x0000	Not used, must be 0x0000
ADC_FILT_COEFF	RAM				ADC filter coefficients, different for 8 k sample/s and 16 k sample/s
		0xC0	[15:0]	0x0000	Not used, must be 0x0000
		0xC1	[15:0]	0x4944	INTERNAL_S0: 8k = 0x4944, 16k = 0x4944
		0xC2	[15:0]	0x4947	INTERNAL_S1: 8k = 0x4947, 16k = 0x4947
		0xC3	[15:0]	0x4343	INTERNAL_S2: 8k = 0x4343, 16k = 0x4343
		0xC4	[15:0]	0x0D45	COEFF_FEDSH: 8k = 0x0D45, 16k = 0x0D25
		0xC5	[15:0]	0x394A	COEFF_D_A0: 8k = 0x394A, 16k = 0x394A
		0xC6	[15:0]	0x5429	COEFF_D_B1: 8k = 0x5429, 16k = 0x5429
		0xC7	[15:0]	0x22C0	COEFF_D_B2: 8k = 0x22C0, 16k = 0x22C0
		0xC8	[15:0]	0x4DF5	COEFF_E_A0: 8k = 0x4DF5, 16k = 0x8C70
		0xC9	[15:0]	0x7363	COEFF_E_B1: 8k = 0x7363, 16k = 0xB5C2
		0xCA	[15:0]	0x4F56	COEFF_E_B2: 8k = 0x4F56, 16k = 0x82F3
		0xCB	[15:0]	0x2BD2	COEFF_E_B3: 8k = 0x2BD2, 16k = 0x4BE5
		0xCC	[15:0]	0x0E0C	COEFF_E_B4: 8k = 0x0E0C, 16k = 0x1969
		0xCD	[15:0]	0x03F8	COEFF_F_A0: 8k = 0x03F8, 16k = 0x03F8
		0xCE	[15:0]	0x057E	COEFF_F_B1: 8k = 0x057E, 16k = 0x057E
		0xCF	[15:0]	0x01B5	COEFF_F_B2: 8k = 0x01B5, 16k = 0x01B5

5.3 DAC registers

Table 7: *Registers for the receive path (DAC), address must be completed with the CODEC number at C_CONFIG_A[11:10] and C_CONFIG_A[9:8] =* '01'

Name	Area	Address [7:0]	Bits	Reset value	Description
DAC_CFG	register	0x01			DAC front-end inverter and sample mode
			[0]	0	C_DA inverter
			[1]	0	Audio signal inverter
			[2]	1	'0' = C_DA changed at rising edge, '1' = C_DA changed at falling edge
			[3]	0	'0' = 8 k sample/s , '1' = 16 k sample/s
			[15:4]	0x000	Not used, must be 0x000
DAC_DIT_CFG	register	0x02	[4:0]	0x01	Dither configuration (optional, must be 0x01)
			[15:5]	0x000	Not used, must be 0x000
DAC_EFB_TYPE	register	0x03	[1:0]	3	Error feedback type of the modulator (optional, must be 3)
			[15:2]	0x0000	Not used, must be 0x0000
DAC_DIT_SH	register	0x04			This register is valid for every CODEC, i.e. any value of address [11:10] accesses the same register.
			[2:0]	0	Dither amplitude shift (optional, must be 0)
			[15:3]	0x0000	Not used, must be 0x0000
DAC_COMP_TYPE	register	0x05			Attenuation versus frequency compensation
			[3:0]	0	Compensation low pass parameter (input shift)
			[7:4]	0	Compensation low pass parameter (feedback shift)
			[8]	0	'0' = compensation disabled, '1' = compensation enabled
			[15:9]	0x00	Not used, must be 0x00
DAC_FILT_COEFF	RAM				DAC filter coefficients, different for 8 k sample/s and 16 k sample/s
		0xC0	[15:0]	0x0000	Offset: 8k = 0x0000, 16k = 0x0000, **offset should be set to** 0x0200
		0xC1	[15:0]	0x1000	DAC_GAIN: 8k = 0x1000, 16k = 0x1000
		0xC2	[15:0]	0x0004	COEFF_GSH: 8k = 0x0004, 16k = 0x0002
		0xC3	[15:0]	0x4DF5	COEFF_G_A0: 8k = 0x4DF5, 16k = 0x8C70
		0xC4	[15:0]	0x7363	COEFF_G_B1: 8k = 0x7363, 16k = 0xB5C2
		0xC5	[15:0]	0x4F56	COEFF_G_B2: 8k = 0x4F56, 16k = 0x82F3
		0xC6	[15:0]	0x2BD2	COEFF_G_B3: 8k = 0x2BD2, 16k = 0x4BE5
		0xC7	[15:0]	0x0E0C	COEFF_G_B4: 8k = 0x0E0C, 16k = 0x1969

5.4 Timing characteristics

Access to registers and RAM have different timing characteristics. Write accesses are shown in Figures 7 and 8 on page 21. Read accesses are shown in Figures 9 and 10 on page 22.

All accesses have in common that the C3-CODEC-G712-4 core operates on rising edges of C_CLK_INTERNAL. For this reason, it is recommended that the external hardware changes input signals (C_CONFIG_A, C_CONFIG_WR, C_CONFIG_DI and C_CONFIG_RD) and samples C_CONFIG_DO on falling edges of C_CLK.

Please note !

There is a two-cycle lock time after every read / write operation for RAM accesses.

Write access

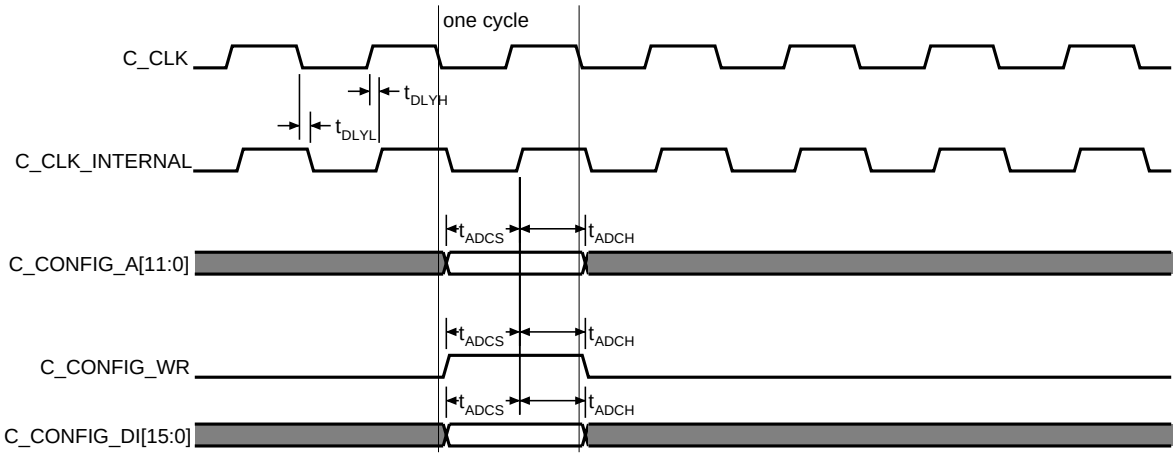

Figure 7: *Register write access*

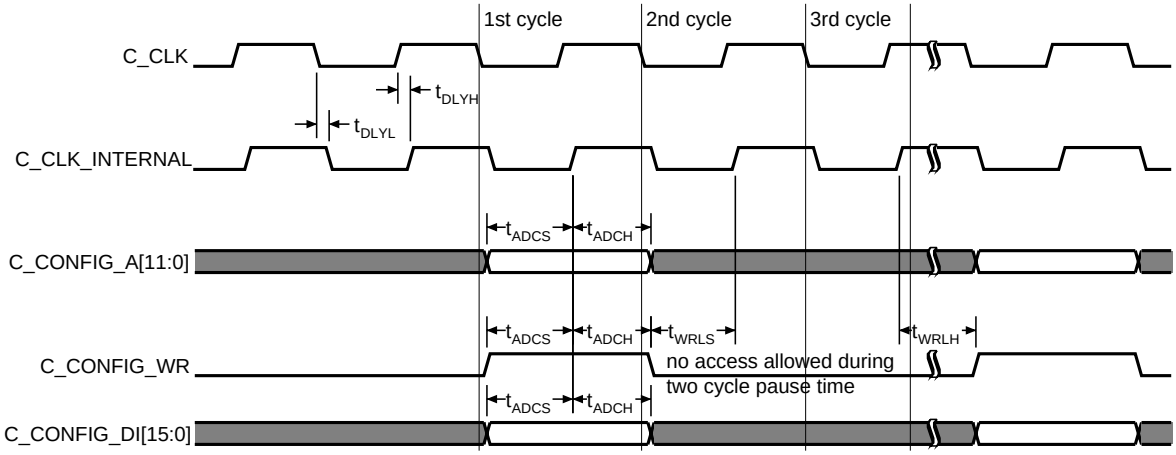

Figure 8: *RAM write access*

Table 8: *Symbols of register write and RAM write accesses in Figures 7 and 8*

Symbol	min / ns	max / ns	Characteristic
t_{DLYL}	0	3	Clock input to internal clock delay (falling edge)
t_{DLYH}	0	3	Clock input to internal clock delay (rising edge)
t_{ADCS}	10		Address, data and control setup time
t_{ADCH}	5		Address, data and control hold time
t_{WRLS}	10		Pause setup time (for RAM access only)
t_{WRLH}	5		Pause hold time (for RAM access only)

Read access

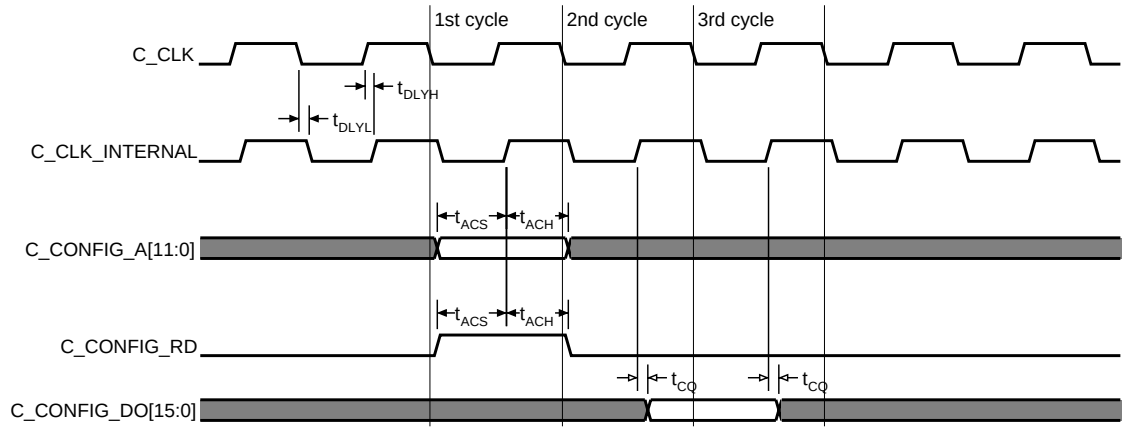

Figure 9: *Register read access*

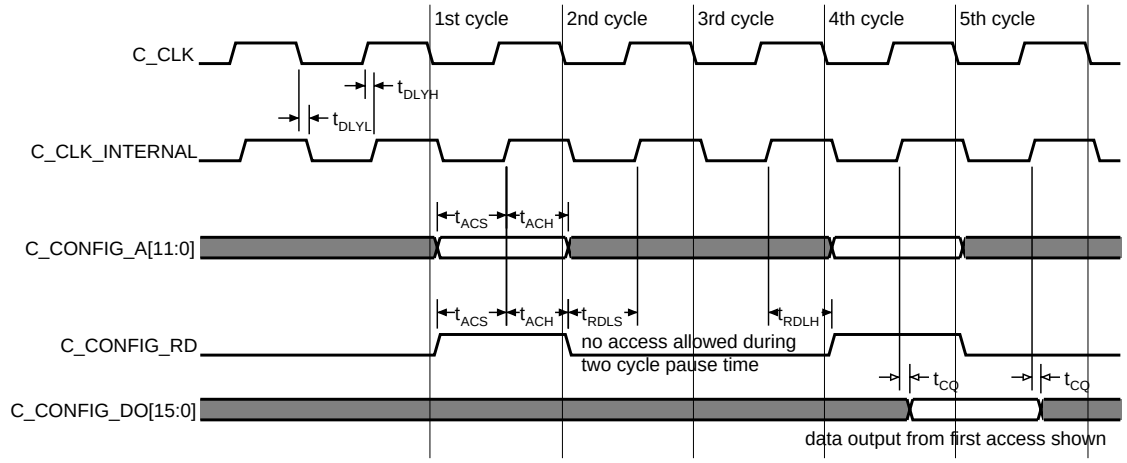

Figure 10: *RAM read access*

Table 9: *Symbols of register read and RAM read accesses in Figures 9 and 10*

Symbol	min / ns	max / ns	Characteristic
t_{DLYL}	0	3	Clock input to internal clock delay (falling edge)
t_{DLYH}	0	3	Clock input to internal clock delay (rising edge)
t_{ACS}	10		Address and control setup time
t_{ACH}	5		Address and control hold time
t_{CQ}	0	1	Internal clock to signal stable delay
t_{RDLS}	10		Pause setup time (for RAM access only)
t_{RDLH}	5		Pause hold time (for RAM access only)

Consecutive access sequences

Figure 11 shows consecutive register and RAM accesses exemplarily for

- a register read access,
- a register write access,
- a RAM read access and
- a RAM write access.

An access is not performed until the previous sequence is finished.

However, accesses can be performed much faster. This is shown in Figure 12 for

- three consecutive register write / read accesses,
- one RAM write / read access and
- two register write / read accesses following.

C_CONFIG_DO shows the valid data output while RD_DATA shows a register which samples C_CONFIG_DO at the falling edge of C_CLK.

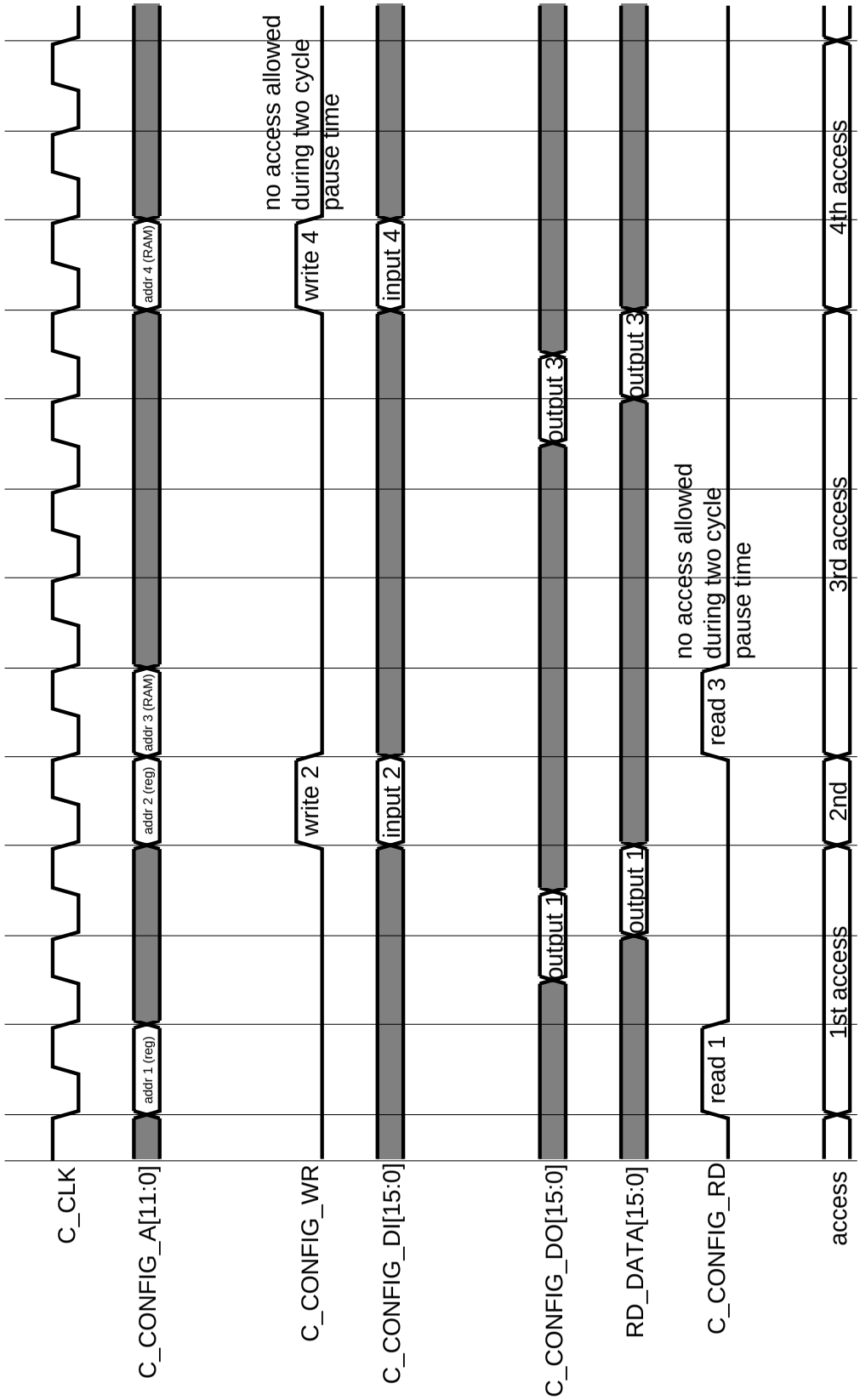

Figure 11: *Slow access sequence*

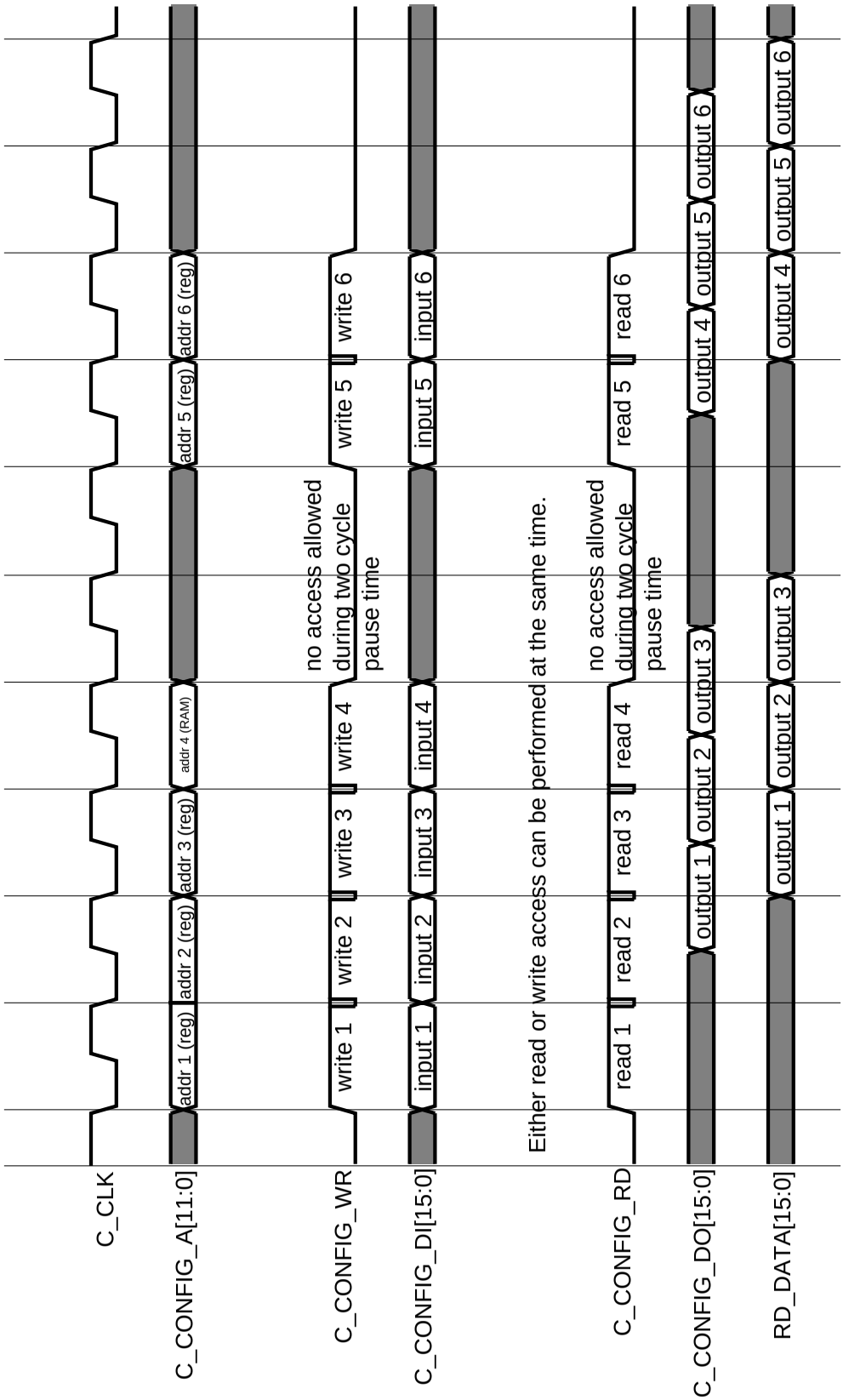

Figure 12: *Fast access sequence*

6 External analog interface and I/O buffers

6.1 External analog ADC circuitry (transmit path)

The external analog ADC circuitry consists of two capacitors and two resistors as shown in Figure 13 exemplarily for CODEC 0. The free terminal of C2 is the single ended input for the analog signal V_{in}.

The feedback loop from AD_I0_EXT to AD_R0_EXT holds the voltage at the capacitor C1 at a fixed level. This level is the switching voltage of the input buffer which is connected to AD_I0_EXT.

The difference between the DC level of the analog input signal V_{in} and this switching level is eleminated by the coupling capacitor C2 in front of the input resistor R2.

When R1 = R2, the maximum peak-to-peak input voltage is $V_{in,max} = 2.2\,\text{V}$ for an input buffer with 3.3 V power supply and a switching threshold of about $0.5V_{dd}$ (in detail, 1.4 V . . 1.9 V for 3.3 V power supply). A different maximum input voltage can be achieved by scaling R1 $\neq$ R2, if desired.

For an input voltage V_{in} with 1.5 V peak-to-peak and R1 = R2, the gain factor ADC_GAIN = 0x1000 (reset default, see Table 6 on page 18) gives a-law / μ-law coded data with about +0dBm0.

6.2 External analog DAC circuitry (receive path)

The external analog DAC circuitry requires only two resistors and three capacitors as shown in Figure 14.

The voltage at C5 is the single ended output V_{out} of the receive path. The attenuation versus frequency characteristic of the DAC is influenced by R3, C3, R4 and C4. The time constants R3 · C3 and R4 · C4 should be about 5 μs to fulfill the ITU G.712 [1] requirement concerning attenuation versus frequency distortion.

A maximum output voltage V_{out} with 1.6 V peak-to-peak can be used for an output buffer with 3.3 V power supply. The gain factor DAC_GAIN = 0x1000 (reset default, see Table 7 on page 19) gives an output voltage range of about 1.1 V peak-to-peak for a-law / μ-law coded data of +0dBm0.

The DC level of DA_0_EXT is approximately $0.5V_{dd}$ for a digital data stream at C_DI which is free from DC.

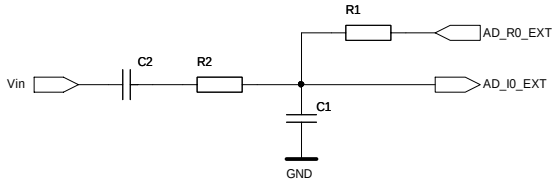

Figure 13: *External ADC circuitry, exemplarily shown for CODEC 0*

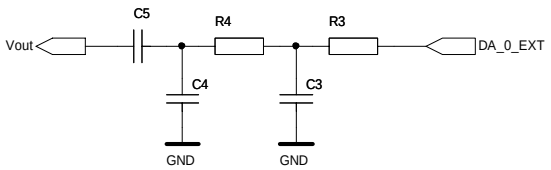

Figure 14: *External DAC circuitry, exemplarily shown for CODEC 0*

6.3 Circuitry version with standard internal I/O buffers

The C3-CODEC-G712-4 needs three standard buffers within the microchip and three additional buffers as external circuitry for every CODEC. This is shown in Figure 15. Standard buffers can be used inside the microchip. The hysteresis of the input buffer should be as small as possible.

It is strongly recommended to provide a dedicated power supply VDD_BUF for every CODEC. The supply voltages should be stabilized to fulfill the ITU G.712 [1] requirements.

The DC level of VDD_BUF defines the level of both the ADC and the DAC audio data:

- The level of the analog output signal Vout is proportional to the power supply level VDD_BUF.
- The ADC data stream is proportional to the input voltage Vin and to the ratio R1/R2, and it is inversely proportional to the buffer supply voltage VDD_BUF.

VDD_BUF must be free from low frequency distortion in the audio band. A low noise level is required because this is added to the input noise at AD_I0_EXT which is used to hold the capacitor C1 at a constant level.

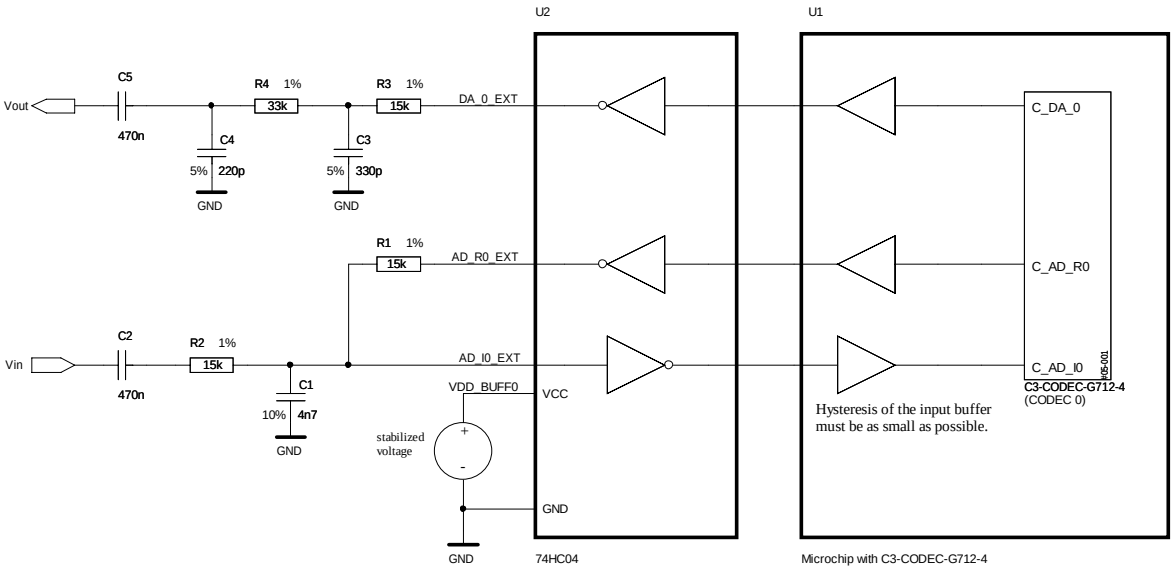

Figure 15: *74HC04 buffer connection to the C3-CODEC-G712-4 core, exemplarily shown for CODEC 0*

> **Please note !**
>
> Every CODEC should have its own 74HC04 device.

6.4 Circuitry version with customized internal I/O buffers

Alternatively, an external circuitry without 74HC04 buffers is avaliable as shown in Figure 16. This circuitry requires customized internal I/O buffers which characteristics are described below.

It is strongly recommended to have separate power supply pins for the buffer group of every CODEC which is isolated from each other and from the common power rail.

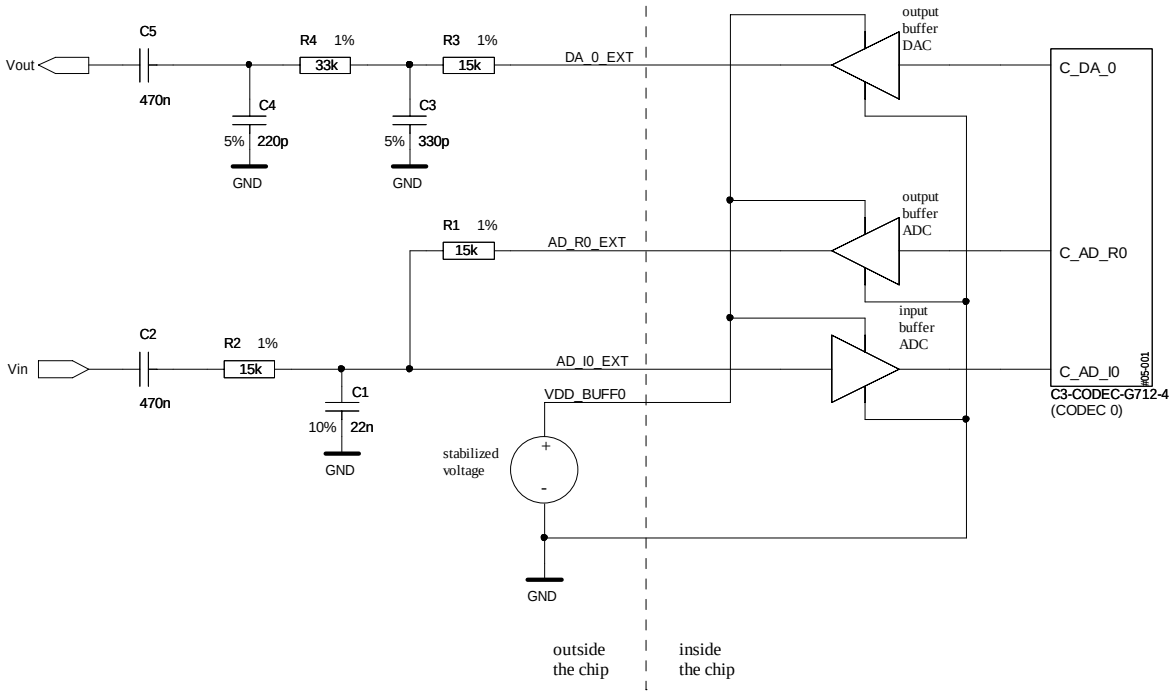

Figure 16: *Buffer connection to the C3-CODEC-G712-4 core, exemplarily shown for CODEC 0*

Input buffer

There is always a current inside the buffers because they are permanently working at their switching level. This current should be minimized using input buffers which have CMOS transistors with small width. No hysteresis or Schmitt-Trigger characteristic is allowed for this buffer.

Even though the slew rate at capacitor C1

$$\frac{dU(\mathrm{C1})}{dt} = \frac{V_{DD}}{2} \cdot \frac{1}{\mathrm{C1} \cdot \mathrm{R1}} = 5\,\mathrm{mV}/\mu\mathrm{s}$$

is quite low, the propagation delay of the input buffer should not exceed 50 ns. Please note, that the capacitor C1 differs to the standard circuitry shown in Figure 15.

Output buffers

The resistance of the output buffers connected to pins C_AD_R and C_DA should be small against the values of R1 and R3 (see Figures 13 and 14). Slew rate controlled buffers are recommended to minimize high frequency coupling effects to other output buffers.

6.5 FPGA implementation with external I/O buffers

As the C3-CODEC-G712-4 core is fully digital, it is implementable in FPGA technology. Standard RAM blocks can be used for the C3-CODEC-G712-4. They can easily be found in every FPGA technology.

Figure 17 shows the external circuitry for C3-CODEC-G712-4 in FPGA implementation. It is the same as Figure 15. The FPGA version can be used for prototyping, for example.

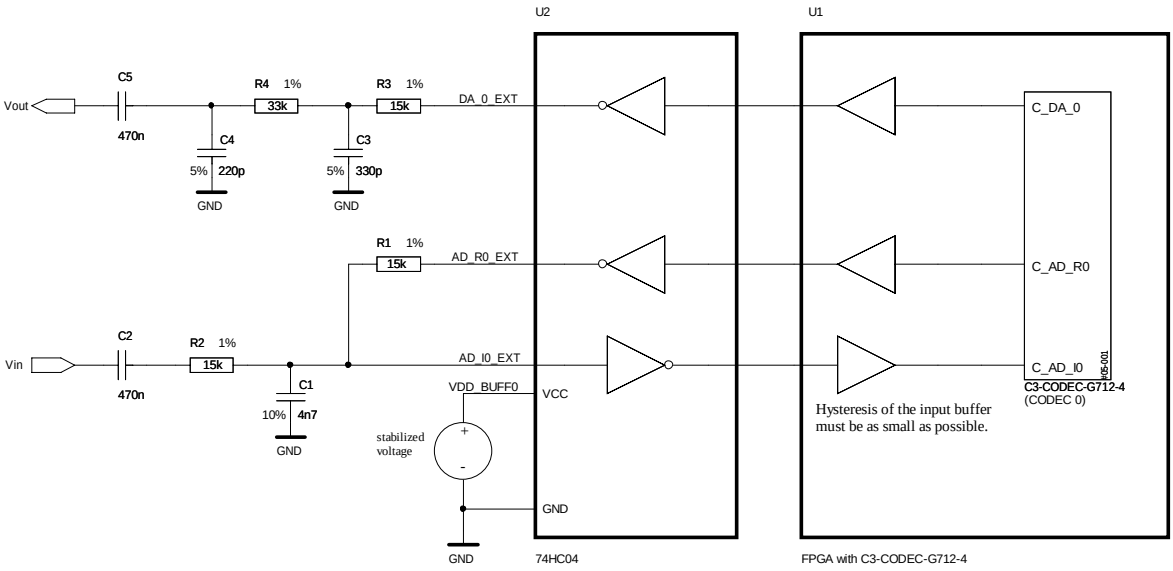

Figure 17: *74HC04 buffer connection to the C3-CODEC-G712-4 core implemented in FPGA technology, exemplarily shown for CODEC 0*

> **Please note !**
>
> Every CODEC should have its own 74HC04 device.

7 Measurements

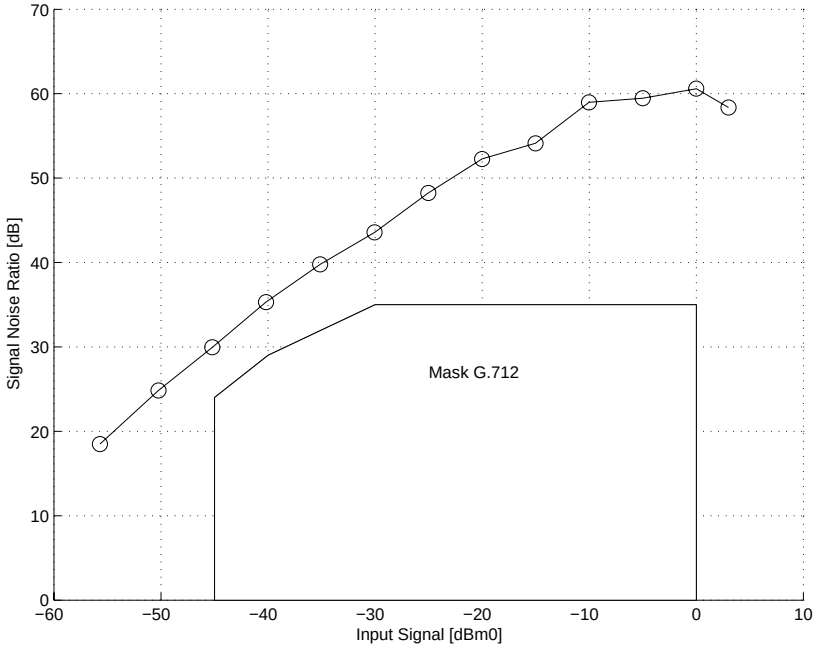

Figure 18: *Signal-to-noise distortion of the ADC*

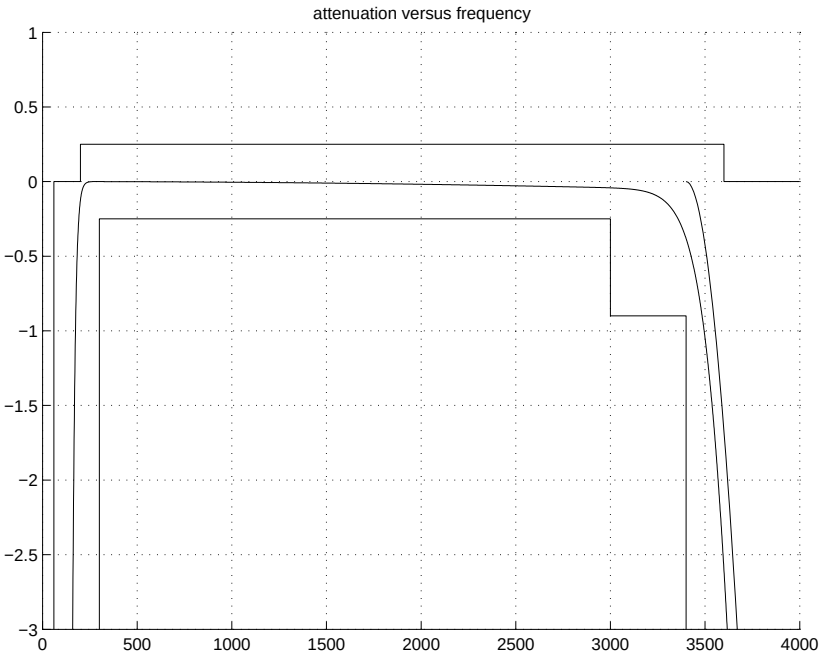

Figure 19: *Filter characteristic of the ADC in the amplitude range +1 . . -3 dB*

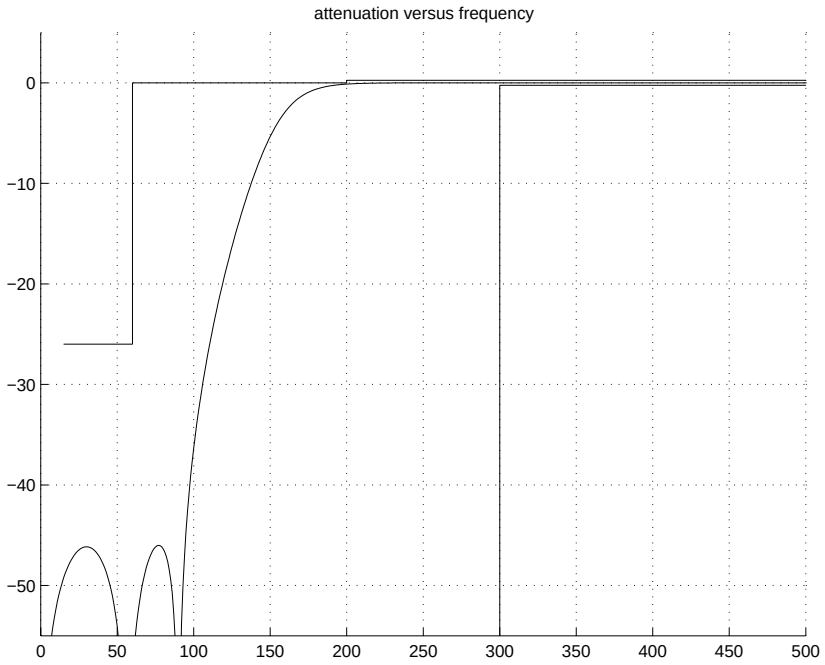

Figure 20: *Filter characteristic of the ADC in the frequency range 0 . . 500 Hz*

8 Deliverables

The C3-CODEC-G712-4 core is available as either Verilog code (RT Level) or a compiled Verilog netlist for the target technology.

To support simulation, a module is available which contains a behavioral model of the external analog circuitry. This module allows interfacing the three signals C_AD_I, C_AD_R and C_DA to an audio stream in a pure digital simulation. The input and output audio data format is 16 bit representing the audio data with a sample rate of 64 kHz.

The C3IP can be obtained directly at Cologne Chip. Please contact our Support Team at support@colognechip.com.

The business model for C3IP depends on the specific customer case. It could be for example a general licence for a semiconductor company, a one time licence for an ASIC project or a royalty based model for design houses.

References

[1] The International Telegraph and Telephone Consultative Committee (CCITT), International Telecommunication Union (ITU). *CCITT G.712: General Aspects of Digital Transmission Systems; Terminal Equipments. Transmission Performance Characteristics of Pulse Code Modulation*, 1992.

[2] The International Telegraph and Telephone Consultative Committee (CCITT), International Telecommunication Union (ITU). *CCITT G.711: General Aspects of Digital Transmission Systems; Terminal Equipments. Pulse Code Modulation (PCM) of Voice Frequencies*, 1993.

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Data Sheet of C3-CODEC-G712-4