Supported by:



Federal Ministry for Economic Affairs and Energy

on the basis of a decision by the German Bundestag

#### **Novel GateMate FPGA Architecture**





## Novel architecture of GateMate FPGA



Overview

• Double checkerboard architecture:

There are only switch boxes on every second field Big and small switchboxes alternate

- Extremely small LUTs (Look Up Table)
- Cologne Programmable Element (CPE) with the following properties:

8 combinatorial inputs with 7 LUT2 as tree

2 flip-flops or latches

2 routed outputs, 2 outputs for additional functions

2 cascaded, not routed connections in the X and Y directions

very flexible clock routing, plus 4 global clocks

CPE can be configured with 2x 4 inputs or 1x 8 inputs

CPE can be 2-bit full-adder or 2x2 multiplier

- Configuration memory of 8-bit latches leads to low internal routing and low SEU probabilities.
- 12 routing layers simplifies Place & Route software.
- Direction Change Multiplexer allows direction change of a signal in every switchbox



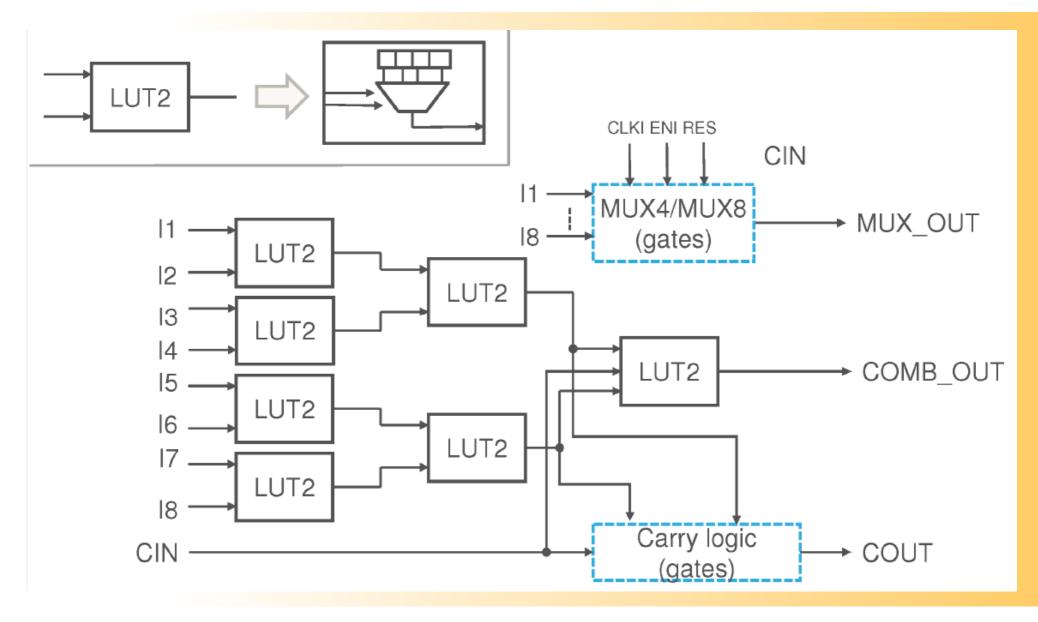
		C	PE			
+	IN1					
	IN2			OU	T2	•
	IN3				τ.	
	IN4 IN5			OU	11	-
	IN6			COUT	Y1	•
	IN7			POUT	Y1	•
•	IN8			COUT	Va	
+	CLK			COUT	A CALENCE	•
+				1 001		
•	EN SR					
	RAM I	2		RAM (	าว	
	RAM I			RAM (	and the second second	-
•	CINX	Σž	2 Z Z	COU	and the second se	•
-	PINX	CINY1 PINY1	<b>PIN</b>	POU	IX	•
		<b>↑ ↑</b>	<b></b>			I

Signals of a CPE (fixed connections in green, RAM-connections in blue)

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#### **CPE combinatorial Part**





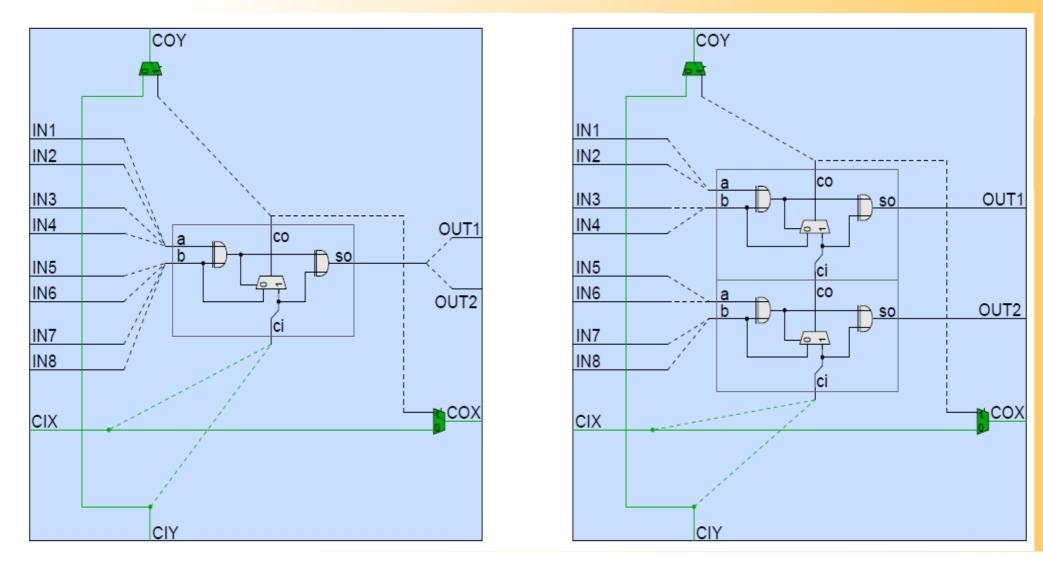
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#### **CPE Fulladder**



#### 1-Bit- und 2-Bit-Fulladder in one CPE



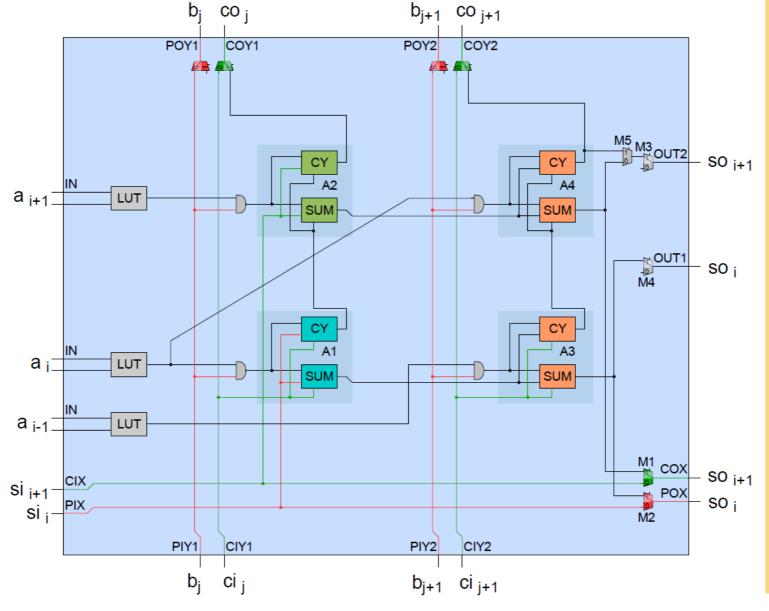
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### **CPE as 2x2 Multiplier block**

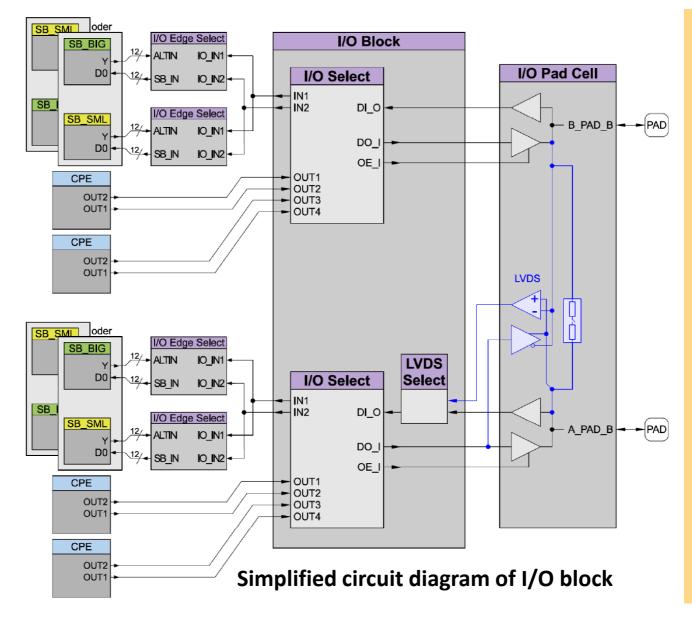




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## I/O Block as Interface to chip outside



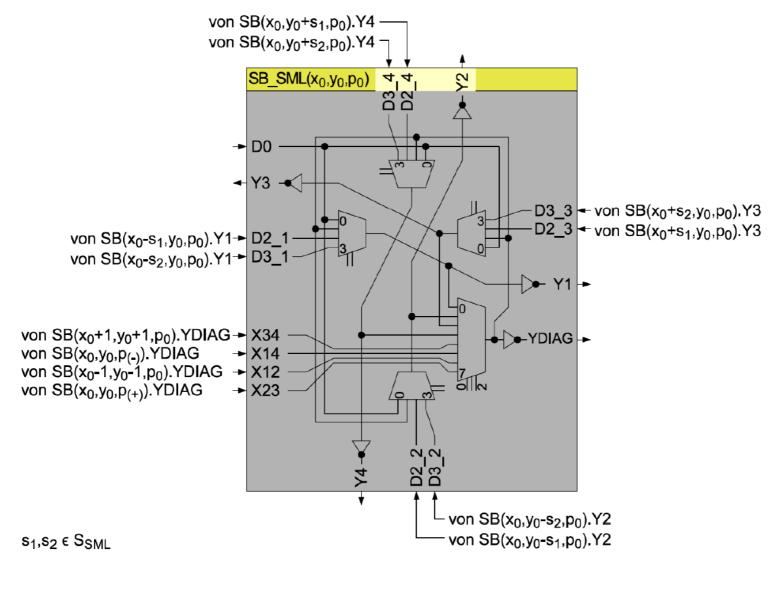


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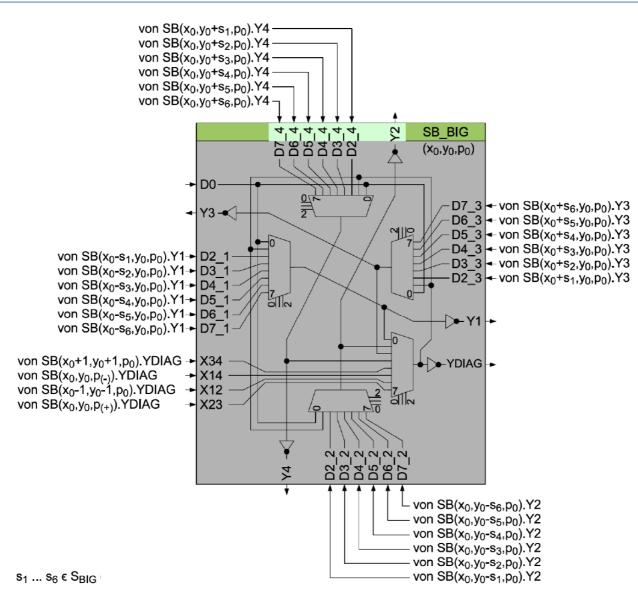
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### Switchbox (small) for Routing

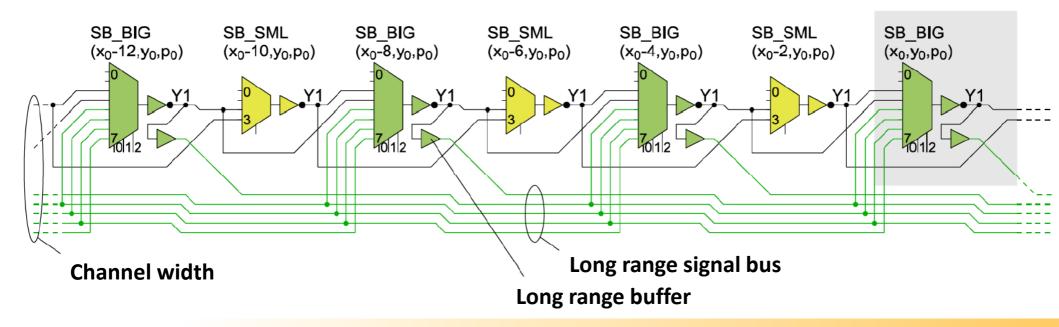


## Switchbox (big) for Routing



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## **Switchbox-Routing in one dimension**

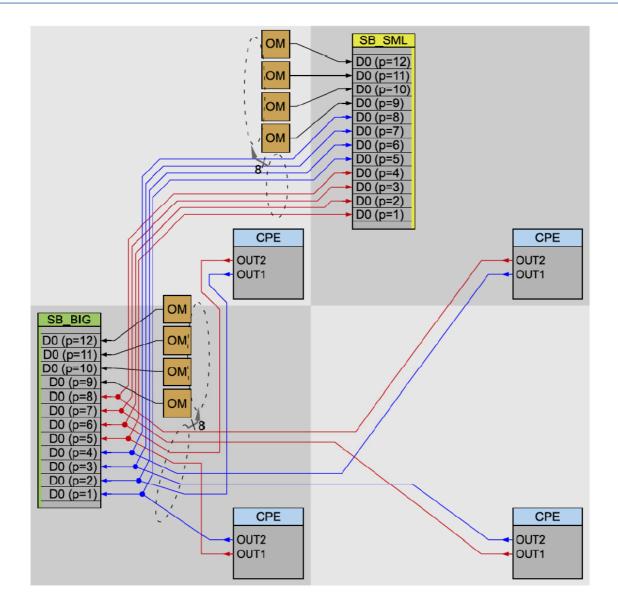


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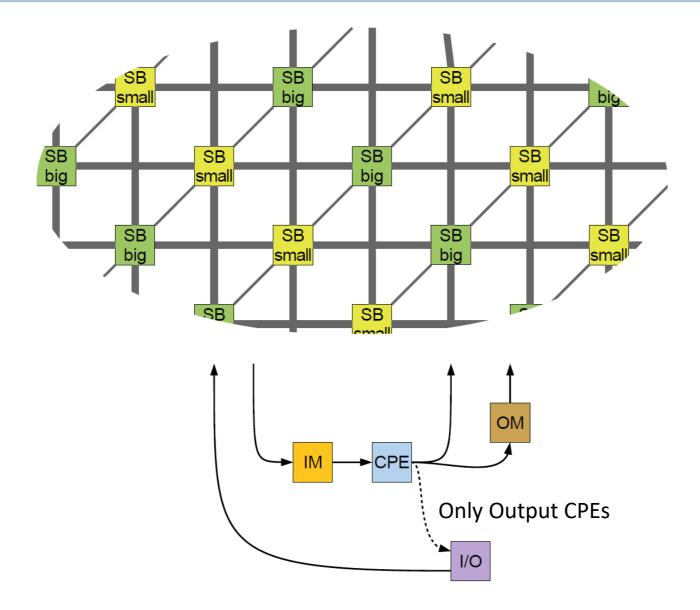
## **Connections of CPEs with Switchboxes**





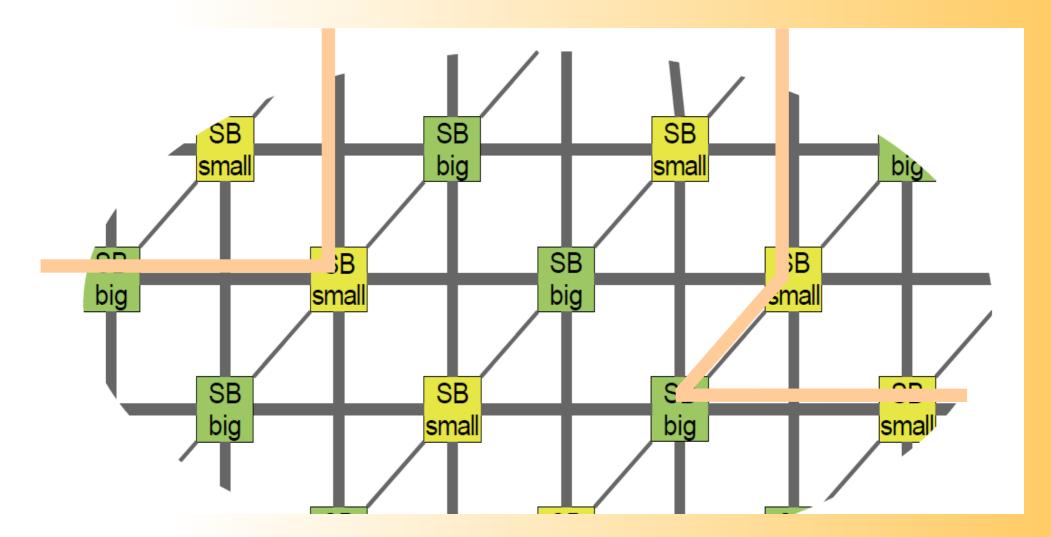
#### **Interaction of FPGA Circuit Elements**





#### **Direction Change via Switch Boxes**

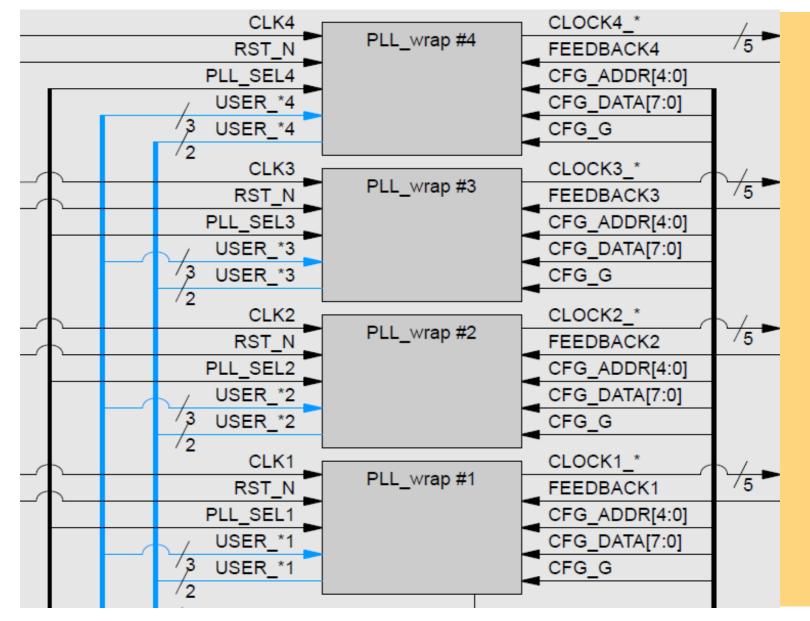




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### **4 general purpose PLL circuits**

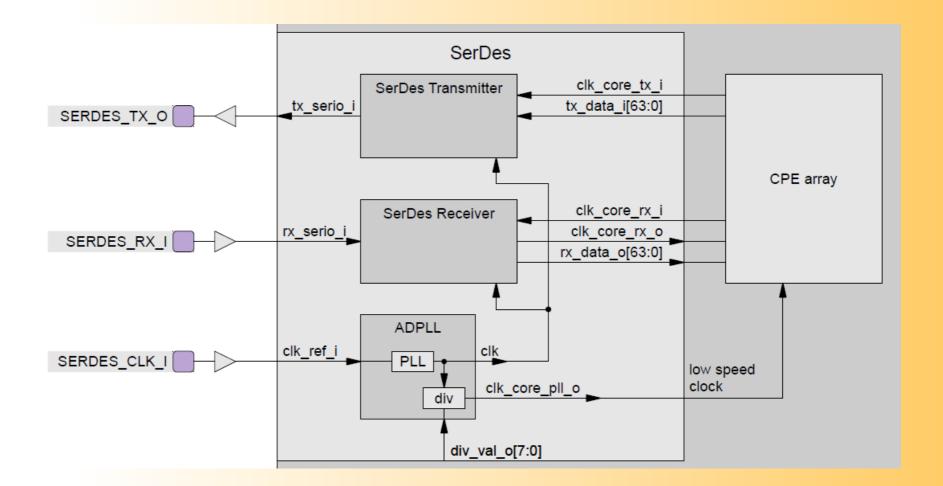




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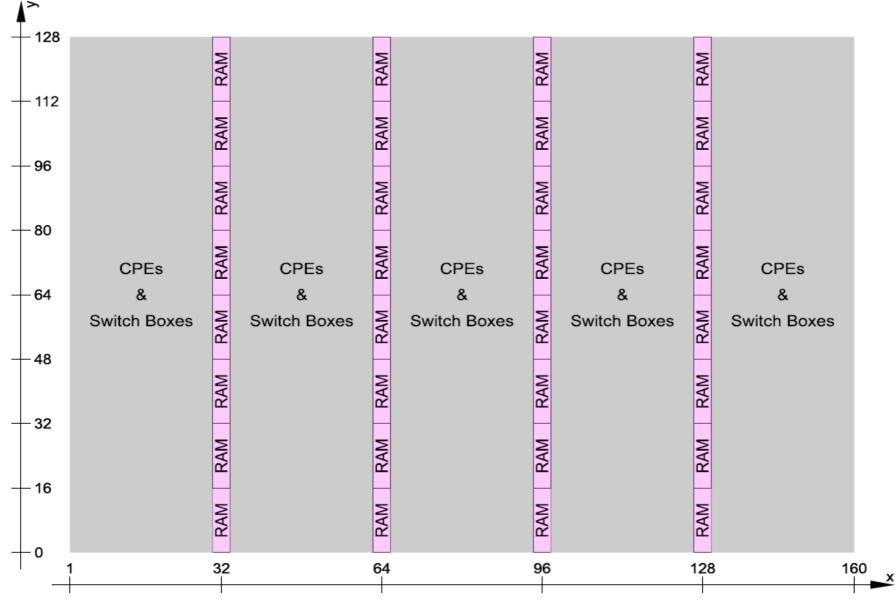
## SERDES high speed interface at 2,5 GBit/s





#### **Dual Port SRAM map**





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## **Dual Port SRAM configuration**



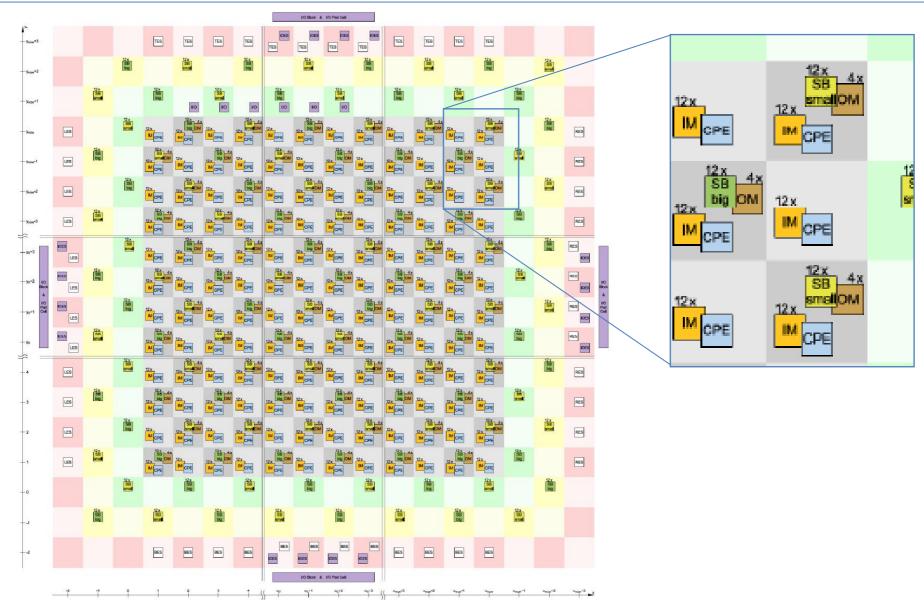
DPSRAM	Non-Split TDP	Non-Split SDP	DPSRAM	Split TDP	Split SDP
configuration	40 Kbit	40 Kbit	configuration	2x20 Kbit	$2 \times 20$ Kbit
$32 \mathrm{K} \times 1 \mathrm{bit}$	$\checkmark$	$\checkmark$	(RAM size per	20 Kbit block	<b>(</b> )
$16 \mathrm{K} \times 2 \mathrm{bit}$	$\checkmark$	$\checkmark$	$16\mathrm{K} \times 1\mathrm{bit}$	$\checkmark$	$\checkmark$
$8\mathrm{K}  imes 5\mathrm{bit}$	$\checkmark$	$\checkmark$	$8 \mathrm{K} \times 2 \mathrm{bit}$	$\checkmark$	$\checkmark$
$4 \mathrm{K} \times 10 \mathrm{bit}$	$\checkmark$	$\checkmark$	$4 \mathrm{K} \times 5 \mathrm{bit}$	$\checkmark$	$\checkmark$
$2 \mathrm{K} \times 20 \mathrm{bit}$	$\checkmark$	$\checkmark$	$2 \mathrm{K} \times 10 \mathrm{bit}$	$\checkmark$	$\checkmark$
$1 \mathrm{K}  imes 40 \mathrm{bit}$	$\checkmark$	$\checkmark$	$1 \mathrm{K}  imes 20 \mathrm{bit}$	$\checkmark$	$\checkmark$
$512  \text{K} \times 80  \text{bit}$	×	$\checkmark$	$512 \mathrm{K} \times 40 \mathrm{bit}$	×	$\checkmark$

#### Every data bit has an own write enable bit

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#### **Overview: Strukture of the FPGA**





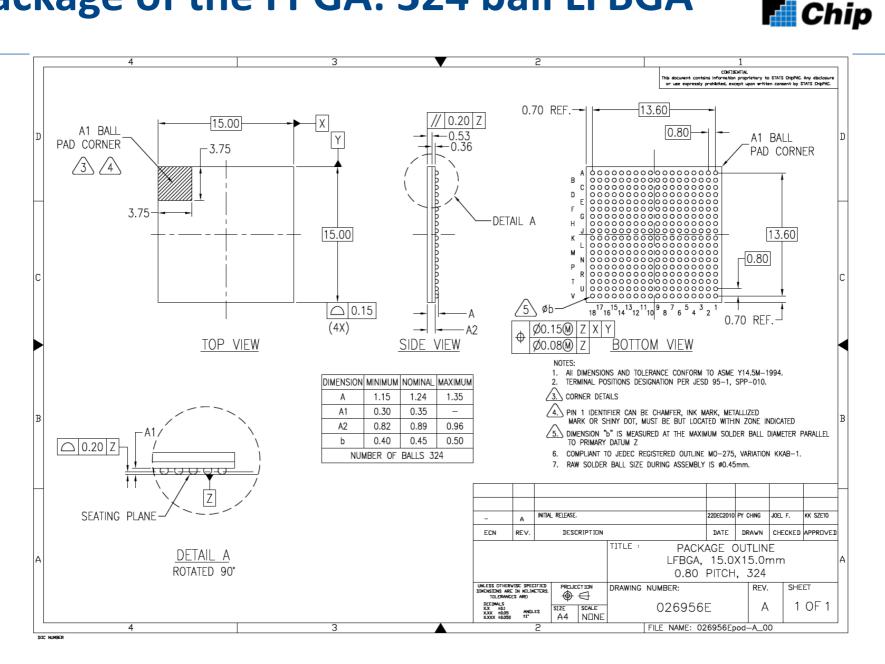
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## **Overall View of the FPGA Die**



																						- L	egend
																							8x8 tile
							Ч								Т						_		DPSRAM 4x512x20
				_		_					-		_		_			_	_				SwitchBox ring around CPE arra
	x 1 x 9 x 17 y 121 y 121 y 121	x 25 y 121 x		x 41 x 4 y 121 y 1	49 x 57 121 y 12	21 ×	x 65 y 121	x 73 y 121	x 81 y 121	x 89 y 121		(97 x (121 y	105 x 121 y	113	x 121 y 121	x	x 129 y 121	x 137 y 121	x 145 y 121	x 153 y 121			PLL
	x1 x9 x17	33	x 33	S	-	65 y					97	5	105 x	-		129 y		-	-	x 153		1 -	Clock wire
	ŷ 113 ŷ 113 ŷ 113	ý 113 <sup>113</sup>	y 113	ŷ 113 ŷ 1				y 113				113 y			y 113	113	y 113	y 113	y 113			_	Crackstop & moisture barrier
	x 1 x 9 x 17 y 105 y 105 y 105	x 25 y 105 x	x 33 y 105	x 41 x 4 y 105 y 1			x 65 y 105	x 73 y 105		x 89 y 105	x 1 97	(97 x 105 y	105 x 105 y	113	x 121 y 105	x			x 145 y 105	x 153 y 105			<ul> <li>Die-2-Die transceivers</li> </ul>
	x1 x9 x17 y97 y97 y97	x 25 97			49 x 5	7 97			x 81	x 89	y 97		105 x					x 137		x 153			<ul> <li>Die-2-Die connections</li> </ul>
<b>-</b> W2		y 97	-	y 97 y			y 97		-	y 97	-	-	-	_	y 97				y 97	y 97	E2		SERDES Phy (RTL frontend)
	x 1 x 9 x 17 y 89 y 89 y 89	x 25 y 89 x 33	x 33 y 89		49 x 5 89 y 8		x 65 y 89			x 89 y 89					x 121 y 89	x 129	x 129 y 89	x 137 y 89	x 145 y 89	x 153 y 89			SERDES Phy (macro)
	x1 x9 x17 y81 y81 y81	x 25 81 y 81	x 33 y 81	x 41 x y 81 y	49 x 5 81 y 8		x 65 y 81			x 89 y 81					x 121 y 81		x 129 y 81	x 137 y 81	x 145 y 81	x 153 y 81			
	x1 x9 x17	x 25	x 33		49 x 5		x 65		-	x 89			105 x	-			_	x 137	x 145	x 153			SERDES associated bondpad
	y 73 y 73 y 73	y 73 X 33	y 73		73 y 7		v 73			v 73		ŷ73 ŷ			y 73	x 129		y 73	y 73	y 73			Ground bondpad VDD core bondpad
	x1 x9 x17 y65 y65 y65	x 25 y 65	x 33 y 65		49 x 5 65 y 6		x 65 y 65			x 89 y 65		x 97 x y 65 y		113 65	x 121 y 65	, 65	x 129 y 65	x 137 y 65	x 145 y 65	x 153 y 65			VDD IO bondpad
	x1 x9 x17	x 25	x 33		49 x 5	7	x 65	x 73	x 81	x 89				113	x 121		x 129	x 137	x 145	x 153		Ê 🗖	VDD Analog bondpad
	y 57 y 57 y 57	y 57 X 33 y	y 57		57 y 5	65 V			-		97 V		-	-	y 57	129 V		y 57		y 57			GPIO/LVDS bondpad
	x1 x9 x17 y49 y49 y49	x 25 y 49	x 33 y 49		49 x 5 49 y 4		x 65 y 49			x 89 y 49				113 49	x 121 y 49	49		x 137 y 49	x 145 y 49	x 153 y 49			Auxiliary IO bondpad (JTAG,SP
-w-1	x1 x9 x17 y41 y41 y41	x 25 y 41 x	x 33 y 41	x 41 x 41 y 41 y	49 x 5 41 y 4	7 1 ×	x 65 y 41			x 89 y 41	x			113	x 121 y 41	x	x 129 y 41	x 137 y 41	x 145 y 41	x 153 y 41			GPIO/LVDS padcell
	x1 x9 x17	33 y x 25 33			49 x 5	65 V			-	_	97 V		-	-		129 y 33	-	x 137	-	x 153	P3 D		VDD core padcell
	y 33 y 33 y 33	y 33		y 33 y		3	y 33	y 33	y 33	y 33	~	y 33 y	33 y	33	y 33	~	y 33	y 33	y 33	y 33			VDD IO padcell
	x 1 x 9 x 17 y 25 y 25 y 25	x 25 y 25 X	x 33 y 25		49 x 5 25 y 2	7 5 x 65	x 65 y 25			x 89 y 25		x 97 x y 25 y		113 25		x		x 137 y 25	x 145 y 25	x 153 y 25			VDD Analog padcell
	x1 x9 x17	x 25 17	× 33		49 x 5	7 y	x 65			x 89	y 17		105 x	113	x 121				x 145	x 153			IO bank with individual IO voltage
		y 17	y 17 x 33	y 17 y	17 y 1 49 x 5		y 17 x 65		-	y 17 x 89			-	-	y 17		y 17 x 129	y 17 x 137	y 17 x 145	y 17 x 153		-	corner cell
	x1 x9 x17 y9 y9 y9	y 9 X 33	y 9	x 41 x y 9 y			y 9			v9			9 y		x 121 y 9	x 129	y 9	y 9	y 9	y 9			
	x1 x9 x17 y1 y1 y1	x 25 1 y 1	x 33 y 1	x 41 x y y	49 x 51 1 y 1		x 65 y 1			x 89 y 1			105 x 1 y		x 121 y 1	y 1	x 129 y 1		x 145 y 1	x 153 y 1			
							2				1			1	T	19							
																ť						N	o. of Die-2-Die (X-dir): 1088
								598un														↓ N	o. of Die-2-Die (Y-dir): 1088

#### Package of the FPGA: 324 ball LFBGA





Cologne



## Package Connections of the FPGA (ball positions and Signal names)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
Α	GND	VDD_ WC	IO_NA _A0	IO_NA _A1	VDD_ NA	IO_NA _A4	GND	IO_NA _A7	IO_NB _B0	GND	IO_NB _B2	IO_NB _B4	GND	IO_NB _B7	IO_EB _B8	VDD_ EB	IO_EB _B5	GND	Α
в	IO_WC _A8	IO_WC _B8	IO_NA _B0	IO_NA _B1	IO_NA _A2	IO_NA _B4	VDD_ NA	IO_NA _B7	IO_NB _A0	VDD_ NB	IO_NB _A2	IO_NB _A4	VDD_ NB	IO_NB _A7	IO_EB _A8	GND	IO_EB _A5	VDD_ EB	в
С	GND	VDD_ WC	IO_WC _A7	IO_WC _B7	IO_NA _B2	IO_NA _A3	10_NA _A5	IO_NA _A6	IO_NA _A8	IO_NB _B1	IO_NB _B3	IO_NB _B5	IO_NB _B6	IO_NB _B8	IO_EB _B7	IO_EB _B6	IO_EB _B4	IO_EB _A4	С
D	IO_WC _A5	IO_WC _B5	IO_WC _A6	IO_WC _B6	VDD_ WC	IO_NA _B3	IO_NA _B5	IO_NA _B6	IO_NA _B8	IO_NB _A1	IO_NB _A3	IO_NB _A5	IO_NB _A6	IO_NB _A8	IO_EB _A7	IO_EB _A6	IO_EB _B2	IO_EB _A2	D
Е	IO_WC _A3	IO_WC _B3	IO_WC _A4	IO_WC _B4	GND	VDD_ NA	GND	VDD_ NA	GND	VDD_ NB	GND	VDD_ NB	GND	VDD_ EB	IO_EB _B3	IO_EB _A3	VDD_ EB	GND	Е
F	GND	VDD_ WC	IO_WC _A2	IO_WC _B2	VDD_ WC	GND	VDD_ NA	GND	VDD	GND	VDD_ NB	GND	VDD_ EB	GND	IO_EB _B1	IO_EB _A1	IO_EB _B0	IO_EB _A0	F
G	IO_WC _A0	IO_WC _B0	IO_WC _A1	IO_WC _B1	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD_ EA	IO_EA _B8	IO_EA _A8	IO_EA _B7	IO_EA _A7	G
н	IO_WB _A7	IO_WB _B7	IO_WB _A8	IO_WB _B8	VDD_ WB	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	IO_EA _B6	IO_EA _A6	VDD_ EA	GND	н
J	GND	VDD_ WB	IO_WB _A6	IO_WB _B6	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD_ EA	IO_EA _B5	IO_EA _A5	IO_EA _B4	IO_EA _A4	J
κ	IO_WB _A5	IO_WB _B5	IO_WB _A4	IO_WB _B4	VDD_ WB	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	IO_EA _B3	IO_EA _A3	IO_EA _B2	IO_EA _A2	κ
L	IO_WB _A3	IO_WB _B3	IO_WB _A2	IO_WB _B2	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD_ EA	IO_EA _B1	IO_EA _A1	VDD_ EA	GND	L
М	GND	VDD_ WB	IO_WB _A1	IO_WB _B1	VDD_ WB	GND	VDD	GND	VDD	GND	VDD	GND	VDD	IO_EA _B0	IO_EA _A0	GND	IO_SB _A3	IO_SB _B3	Μ
Ν	IO_WB _A0	IO_WB _B0	IO_WA _A8	IO_WA _B8	VDD_ WA	VDD	GND	VDD	GND	VDD	VDD_ SB	GND	VDD_ SB	IO_SB _A8	IO_SB _B8	N.C.	GND	VDD_ SB	Ν
Ρ	IO_WA _A7	IO_WA _B7	VDD_ WA	GND	VDD_ WA	VDD_ SA	GND	VDD_ SA	GND	VDD_ SA	IO_SB _A4	IO_SB _A7	IO_SB _B7	IO_SB _A6	IO_SB _B6	VDD_ PLL	IO_SB _A2	IO_SB _B2	Ρ
R	IO_WA _A6	IO_WA _B6	IO_WA _A5	IO_WA _B5	IO_WA _A0	IO_SA _A1	IO_SA _A2	IO_SA _A4	IO_SA _A6	IO_SA _A7	IO_SB _B4	GND	IO_SB _A5	IO_SB _B5	VDD_ SB	GND	IO_SB _A1	IO_SB _B1	R
т	VDD_ WA	IO_WA _A4	IO_WA _B4	GND	10_WA _B0	IO_SA _B1	IO_SA _B2	IO_SA _B4	IO_SA _B6	IO_SA _B7	GND	SER_ CLK	SER_ CLK_N	VDD _CLK	RST_N	VDD_ SER_PLL	GND	VDD_ SB	т
U	IO_WA _A3	IO_WA _B3	VDD_ WA	IO_WA _A1	IO_SA _A0	VDD_ SA	IO_SA _A3	IO_SA _A5	VDD_ SA	IO_SA _A8	SER_ RX_P	VDD_ SER	SER_ TX_P	GND	GND	TEST MODE	IO_SB _A0	IO_SB _B0	U
v	GND	IO_WA _A2	IO_WA _B2	IO_WA _B1	IO_SA _B0	GND	IO_SA _B3	IO_SA _B5	GND	IO_SA _B8	SER_ RX_N	SER_ Rterm	SER_ TX_N	GND	POR_ ADJ	GND	VDD_ SER	GND	V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

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#### **Packaged Sample from MPW-Run**





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#### Manufactured by GLOBALFOUNDRIES in Dresden



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#### Size versions



	Rel. size	Cologne	Programma	ble Elements	Block	RAM	PLLs	SERDES	I/	Os	Package		
		CPEs	8-Inp- LUT tree	FF/Latches	20Kb	40Kb			single- ended	differential	balls	size (mm)	
CCGM1A1	1	20,480	20,480	40,960	64	32	4	1	162	81	324BGA	15x15	
CCGM1A2	2	40,960	40,960	81,920	128	64	8	2	162	81	324BGA	15x15	
CCGM1A4	4	81,920	81,920	163,840	256	128	16	4	162	81	324BGA	15x15	
CCGM1A9	9	184,320	184,320	368,640	576	288	36	9	tbd	tbd	676BGA	27x27	
CCGM1A16	16	327,680	327,680	655,360	1,024	512	64	16	tbd	tbd	676BGA	27x27	
CCGM1A25	25	512,000	512,000	1,024,000	1,600	800	100	25	tbd	tbd	1156BGA	35x35	

# Special Features for reduced cost of ownership



#### Power

- 3 application modes for the same device only by changing core voltage low power, economy, speed
- > low inventory because of same device for many projects
- Only 2 supply voltages needed, can be applied in any order
- No excessive start-up currents
- > low cost voltage regulators usable

#### Package

- Small high ball count packages starting at 15x15mm with 324 balls BGA
- Only 2 signal layers needed on PCB
- > low cost conventional PCB

#### Supply

- Manufactured in Germany by Globalfoundries
- > No unreasonable price rises or tax increase because of trade wars

## Special Features for better performance Cologne

#### 2x/4y Carry/Propagation lines

- High speed lines without routing Switchboxes.
- could be used also for clock and enable signals
- Is used for adders and multipliers

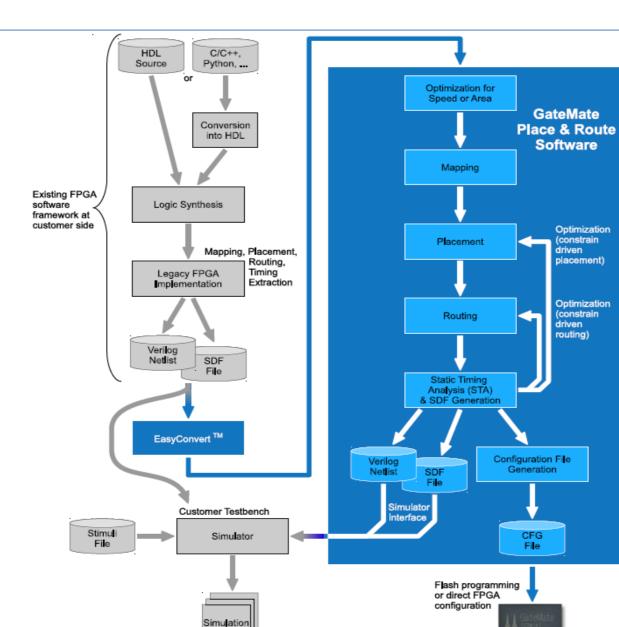
#### Very fast configuration from external low cost Flash memory

- 100 MHz quad mode SPI supported
- Low cost general purpose serial Flash device applicable, no need for special PROMs
- Only those configuration latches really used must be configured
- A1 device can be fully configured in only 55ms

#### **RAM size and orientation**

 Superset of known FPGA architectures with 20/40 Bit data width and WE for every bit

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Results

## **Design flow**





#### Thank you for your attention!



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