Supported by:

Federal Ministry
for Economic Affairs
and Energy

on the basis of a decision
by the German Bundestag

# Novel GateMate FPGA Architecture

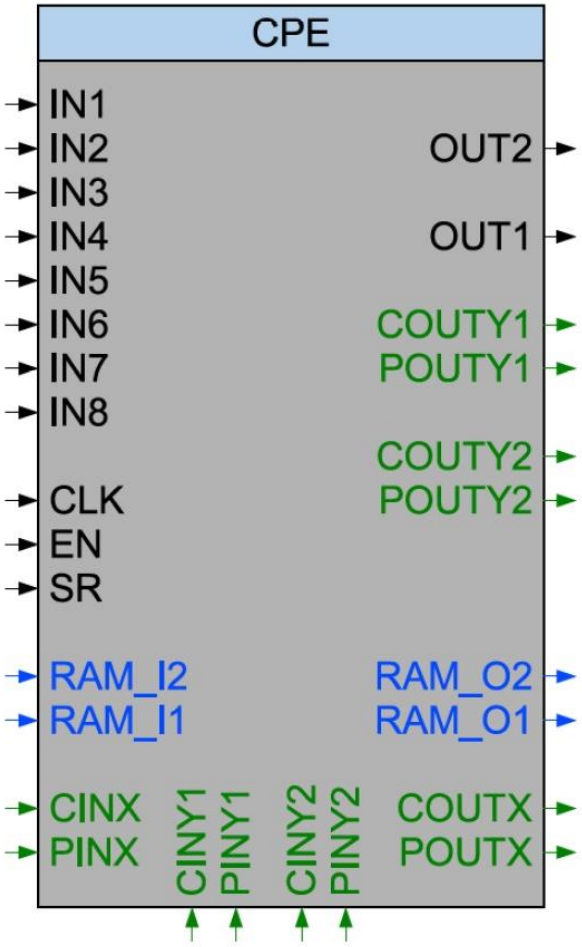

Cologne Chip

# Novel architecture of GateMate FPGA

## Overview

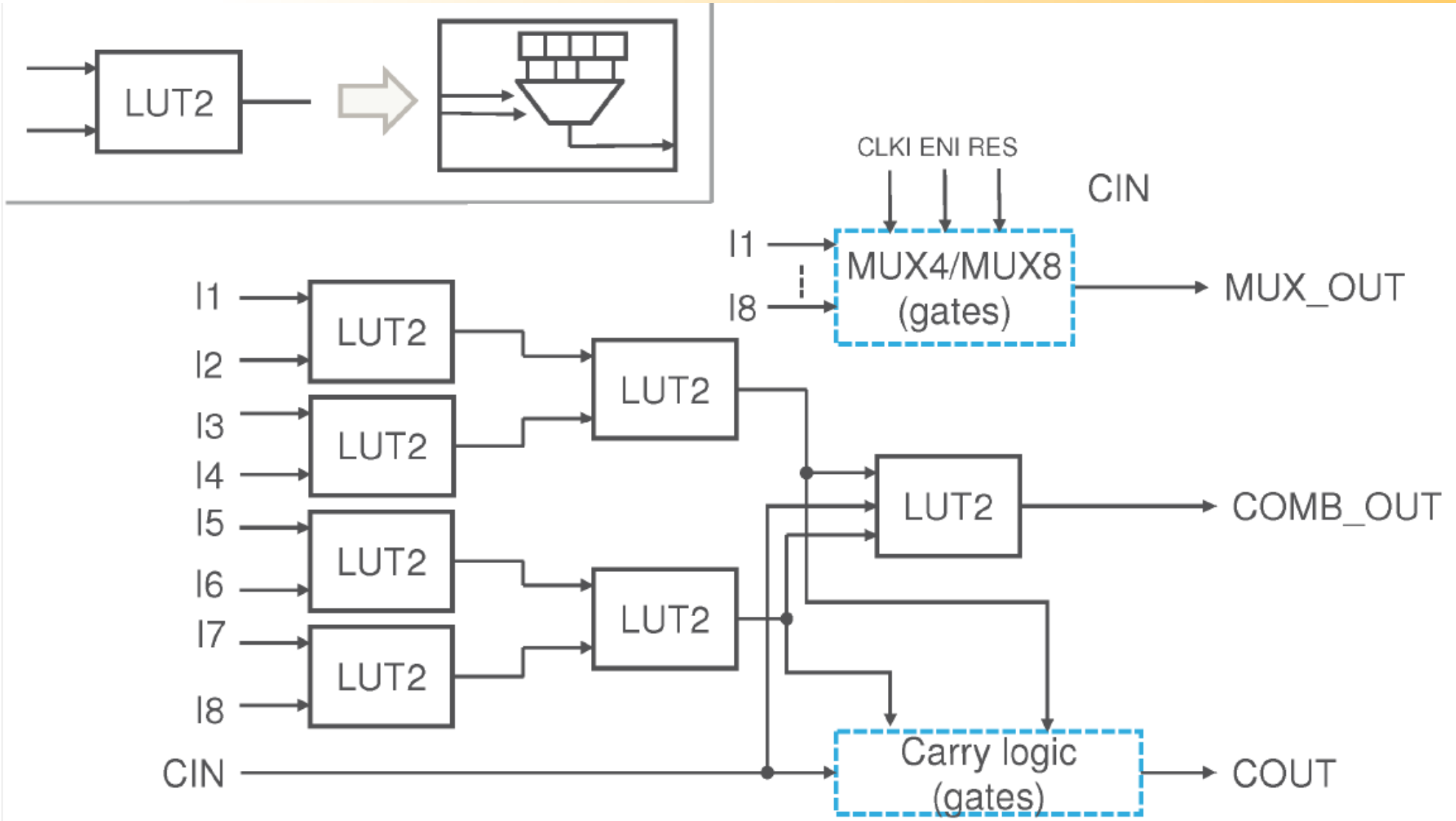
- **Double checkerboard architecture:**
  - **There are only switch boxes on every second field**
  - **Big and small switchboxes alternate**
- **Extremely small LUTs (Look Up Table)**
- **Cologne Programmable Element (CPE) with the following properties:**
  - **8 combinatorial inputs with 7 LUT2 as tree**
  - **2 flip-flops or latches**
  - **2 routed outputs, 2 outputs for additional functions**
  - **2 cascaded, not routed connections in the X and Y directions**
  - **very flexible clock routing, plus 4 global clocks**
  - **CPE can be configured with 2x 4 inputs or 1x 8 inputs**
  - **CPE can be 2-bit full-adder or 2x2 multiplier**
- **Configuration memory of 8-bit latches leads to low internal routing and low SEU probabilities.**
- **12 routing layers simplifies Place & Route software.**
- **Direction Change Multiplexer allows direction change of a signal in every switchbox**

# Cologne Programmable Element (CPE)



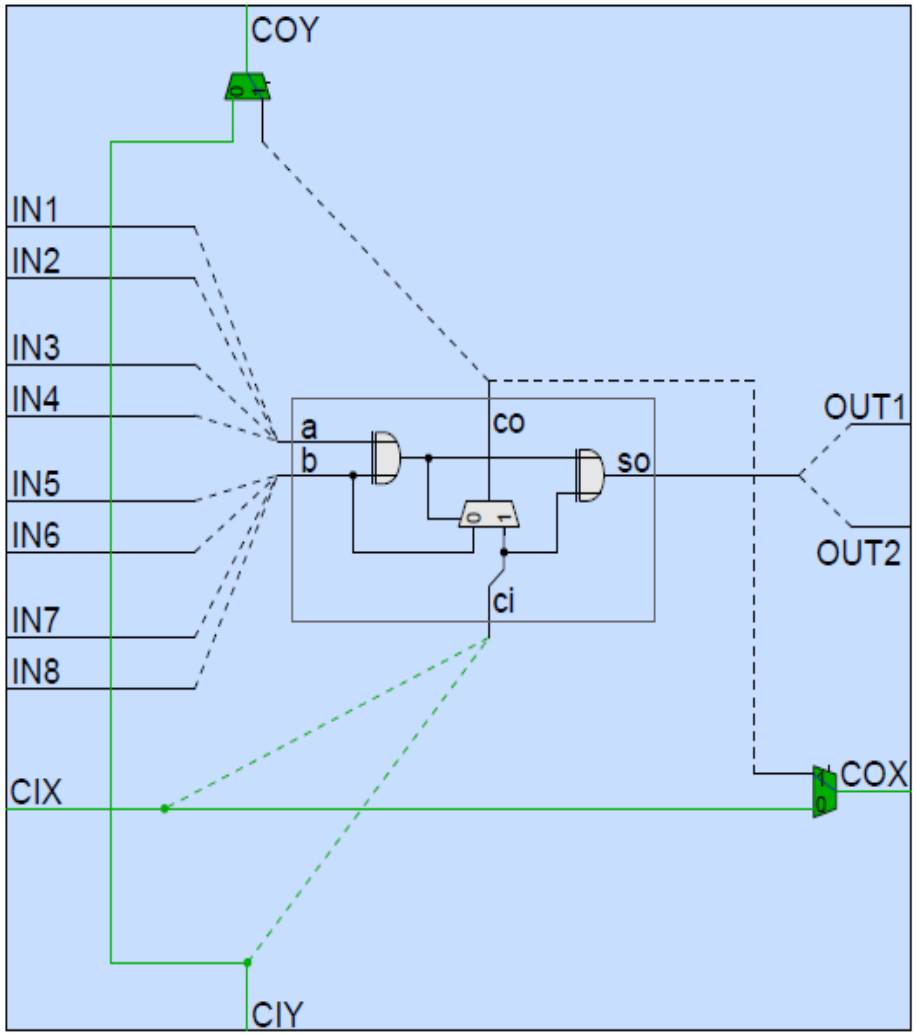

**Signals of a CPE**
**(fixed connections in green,**
**RAM-connections in blue)**

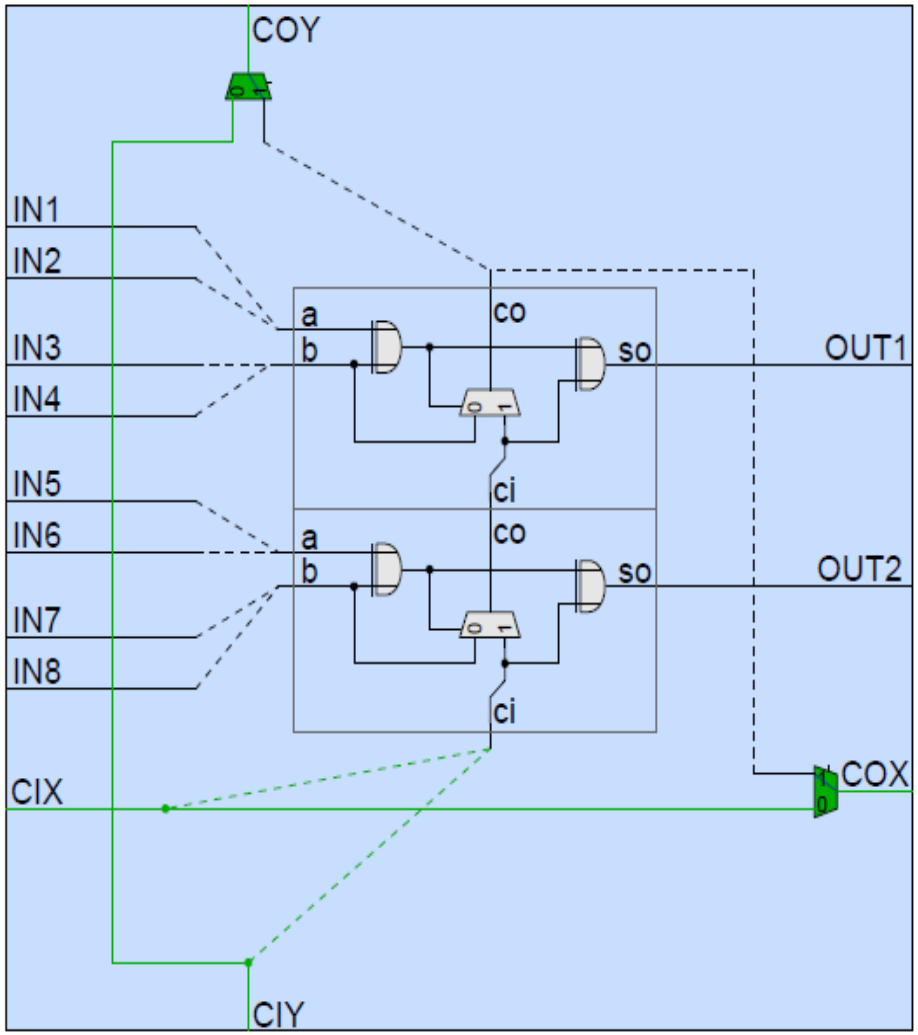
# CPE combinatorial Part



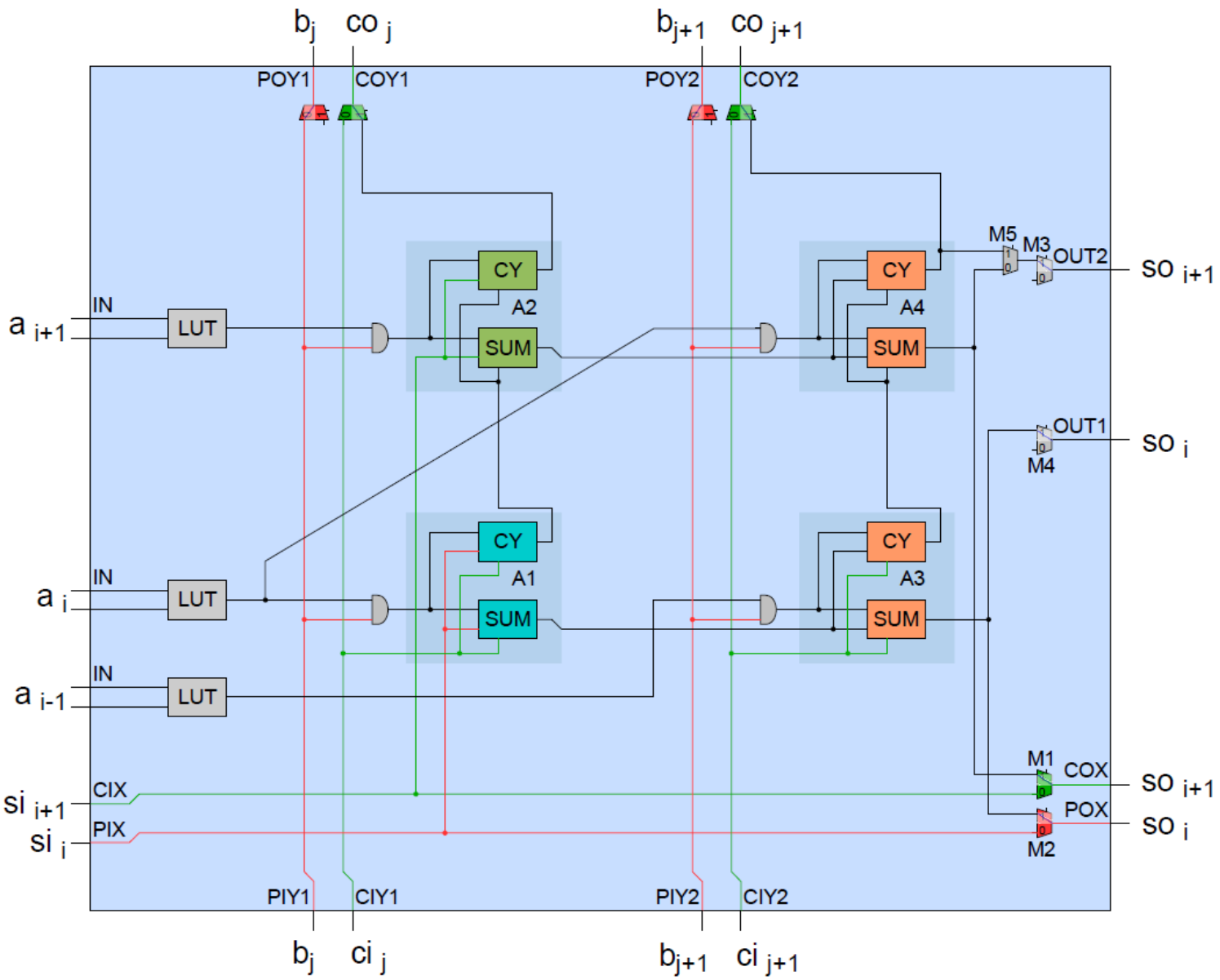
# CPE Fulladder

1-Bit- und 2-Bit-Fulladder in one CPE

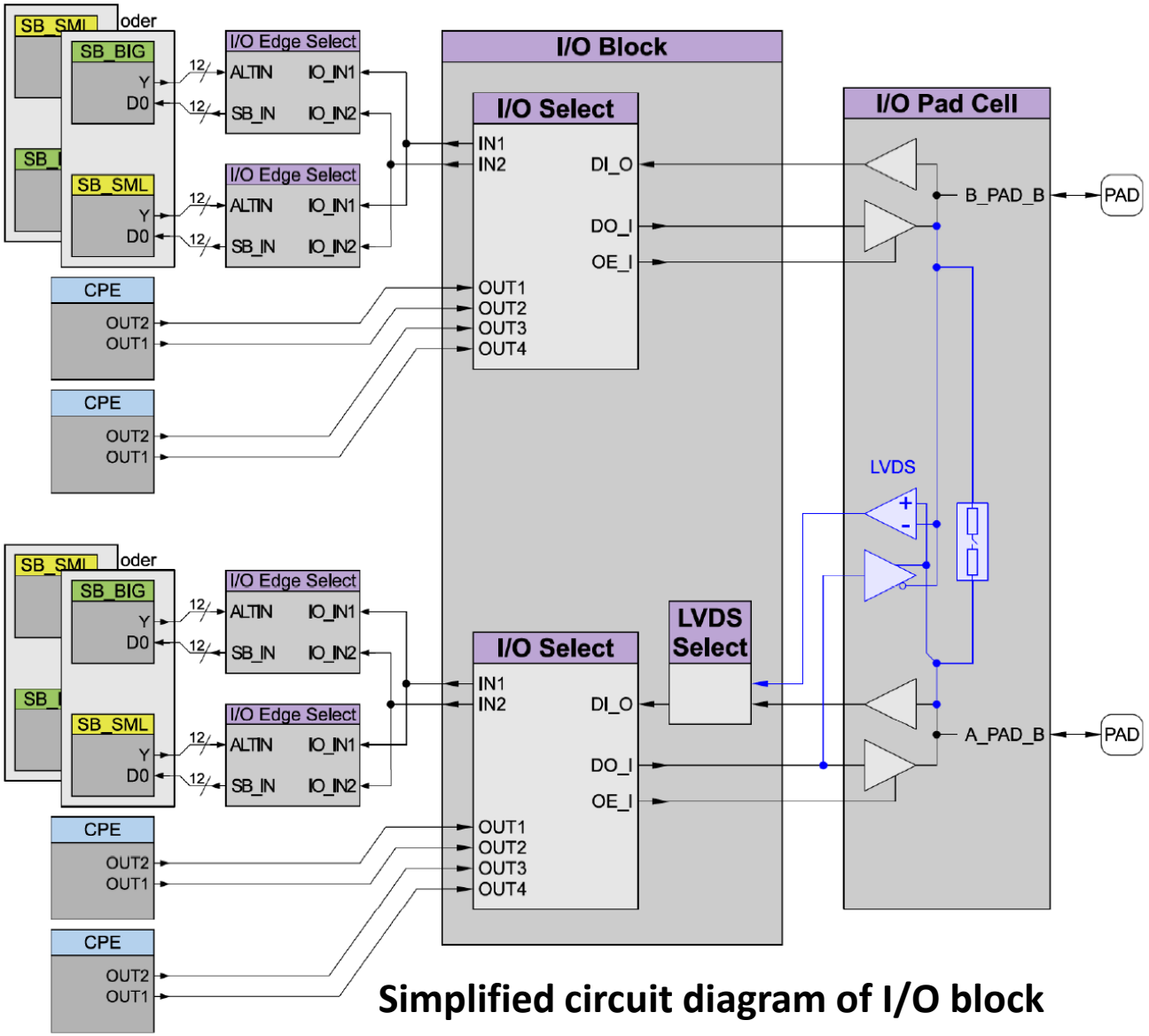


# CPE as 2x2 Multiplier block

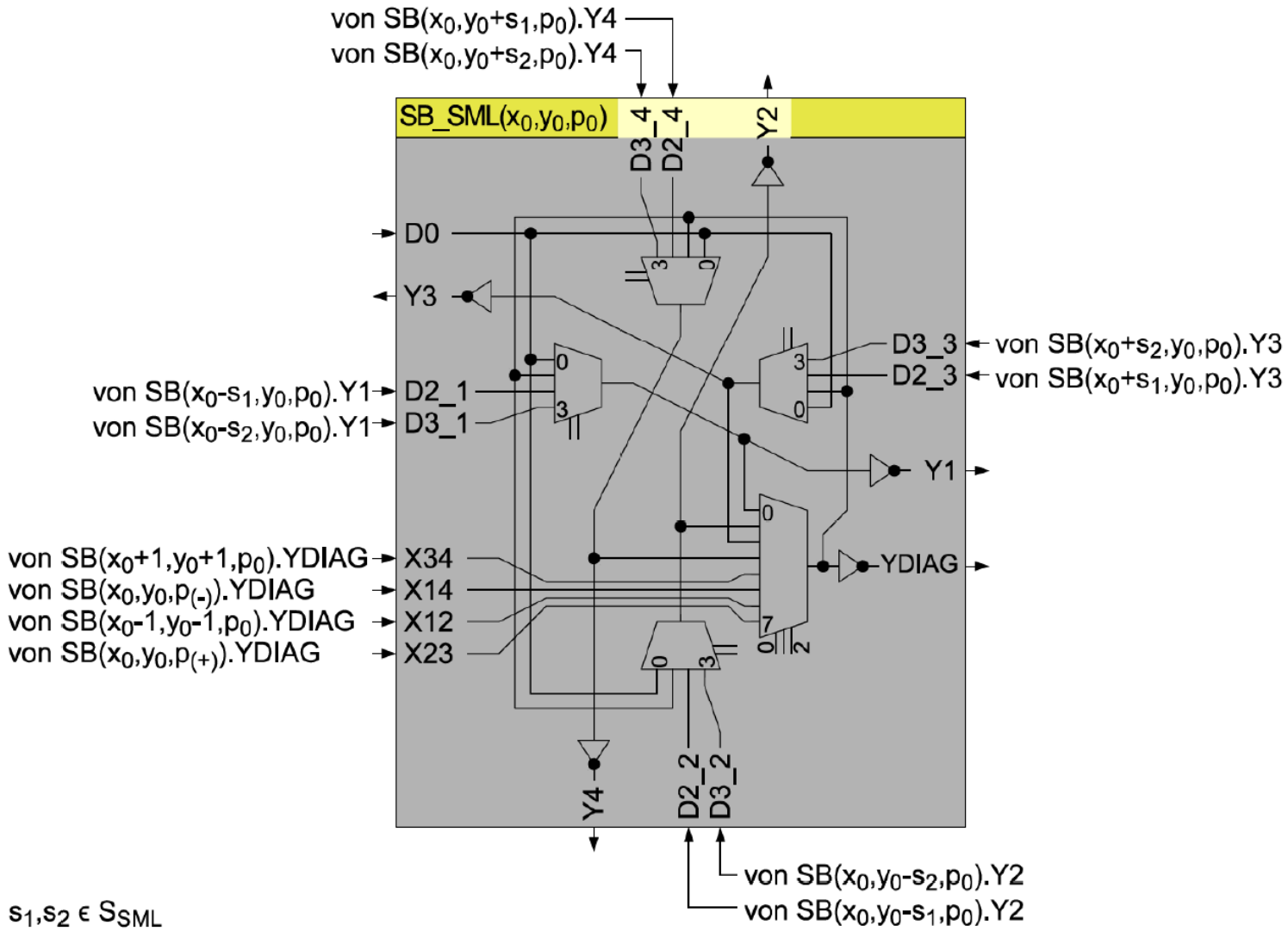


# I/O Block as Interface to chip outside

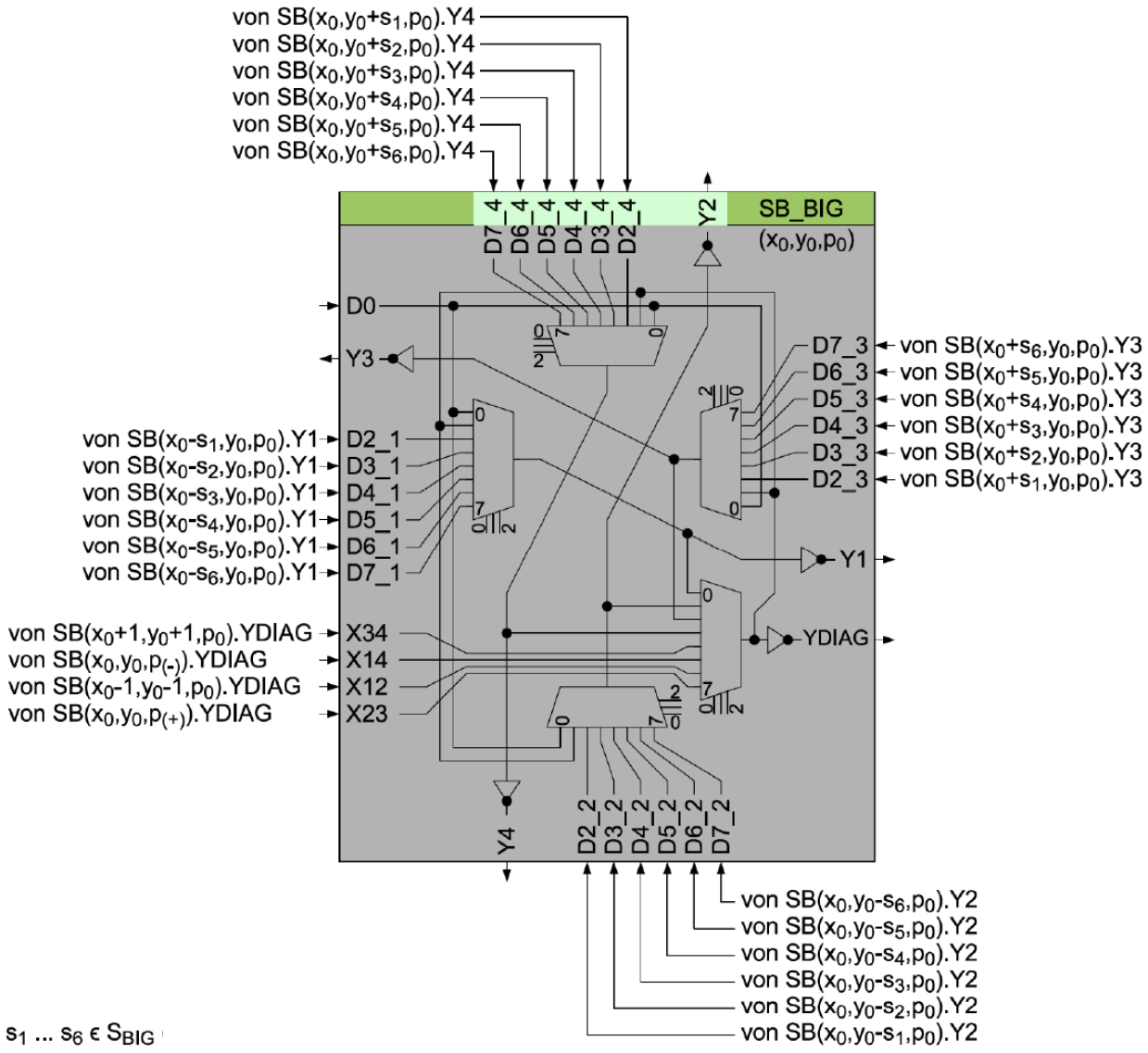



**Simplified circuit diagram of I/O block**

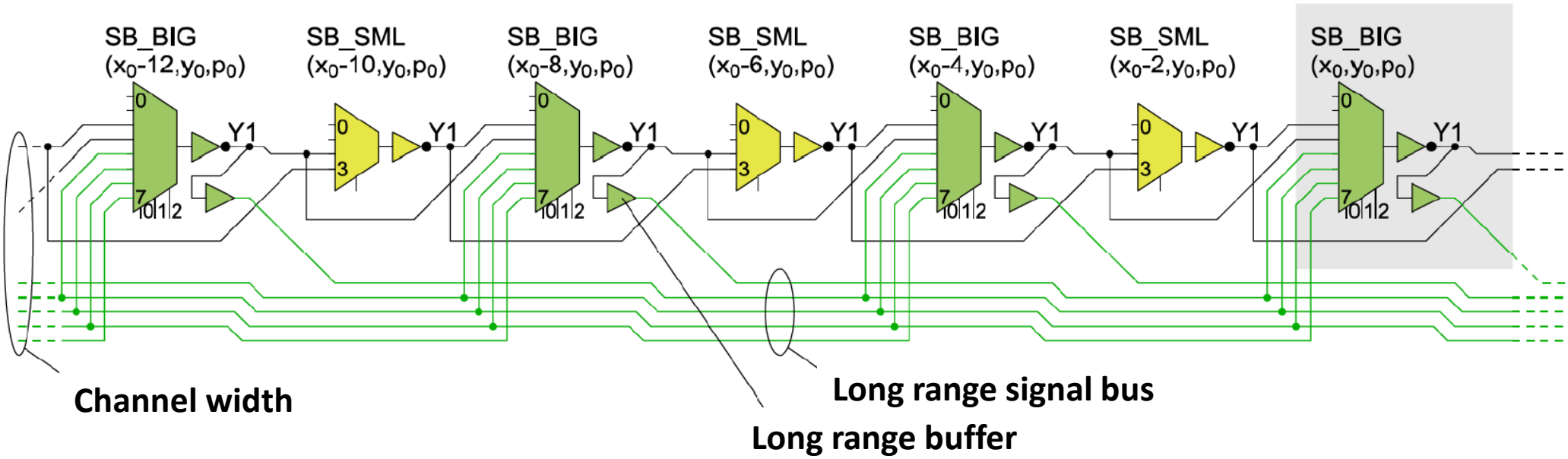
# Switchbox (small) for Routing



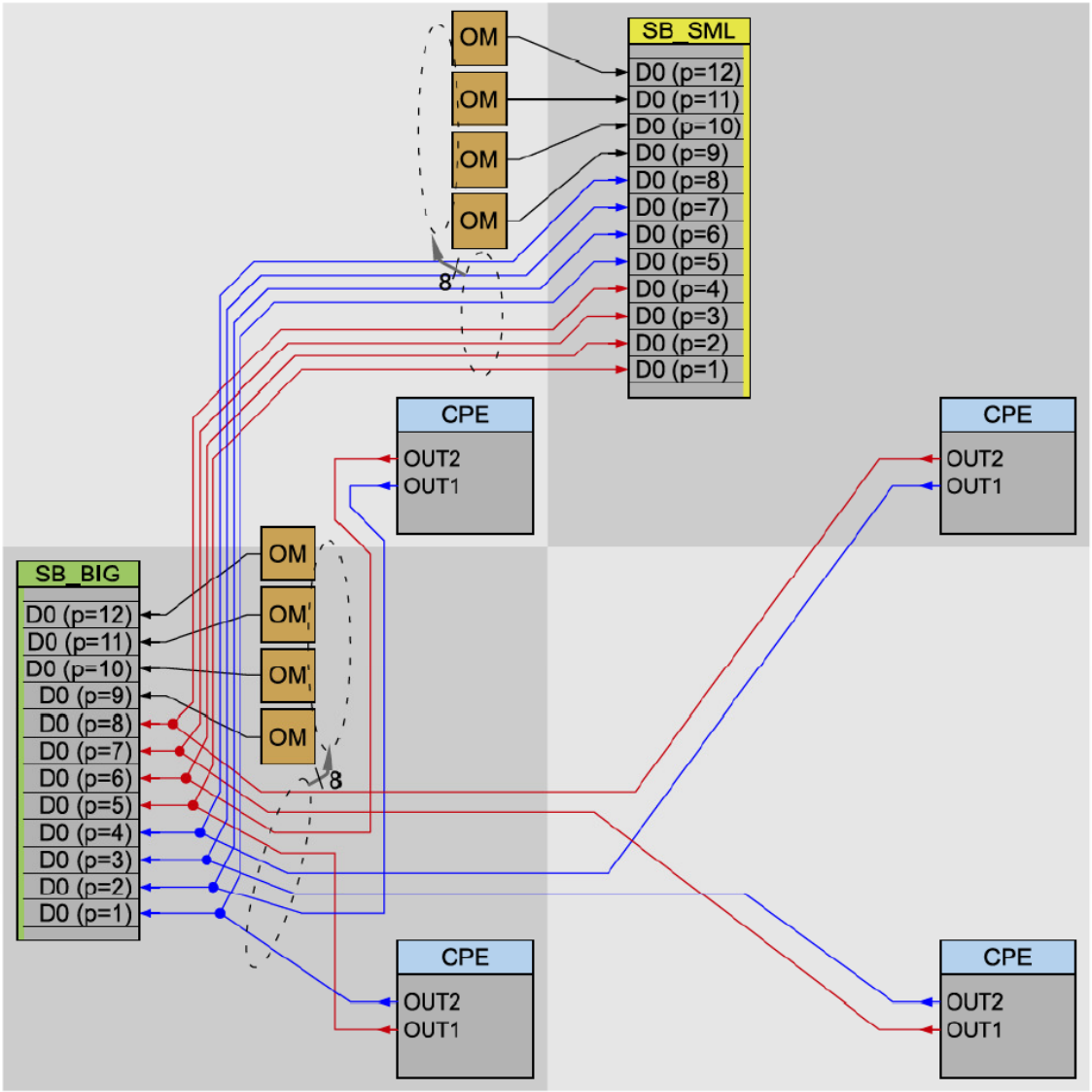
# Switchbox (big) for Routing



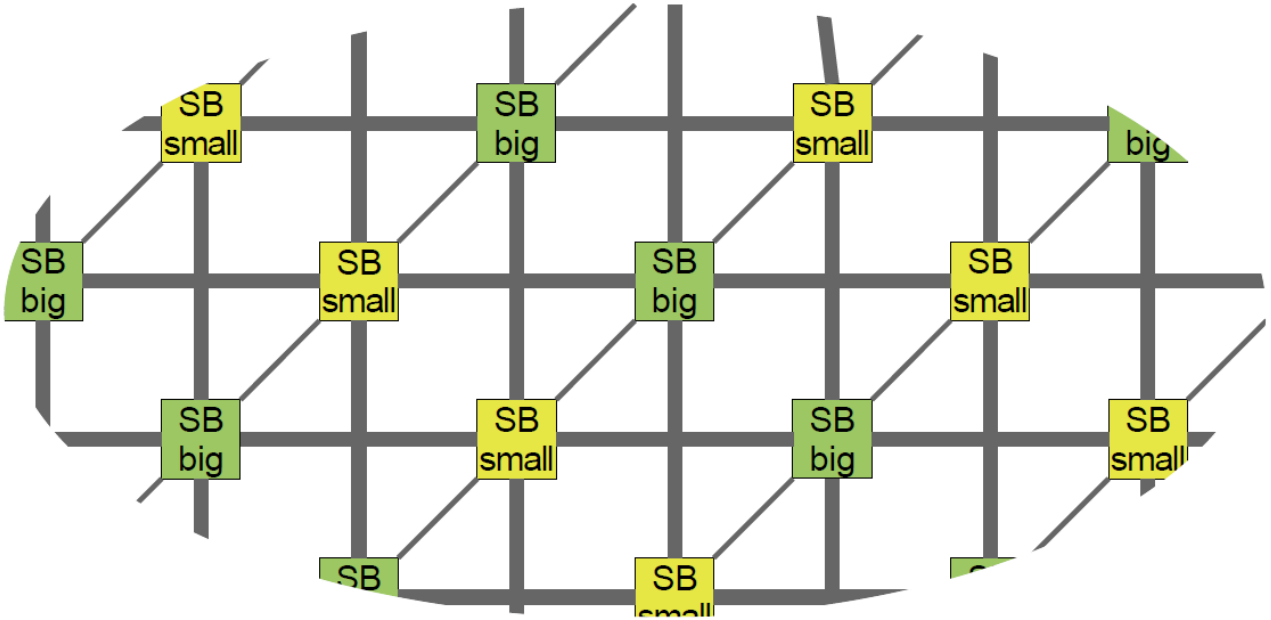
# Switchbox-Routing in one dimension

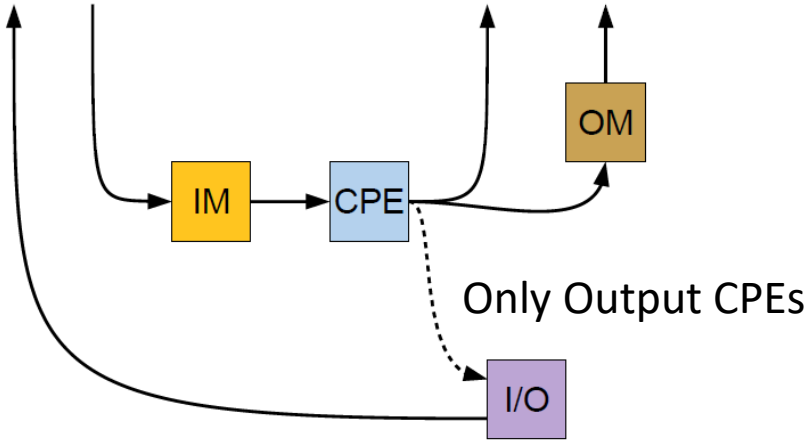


# Connections of CPEs with Switchboxes

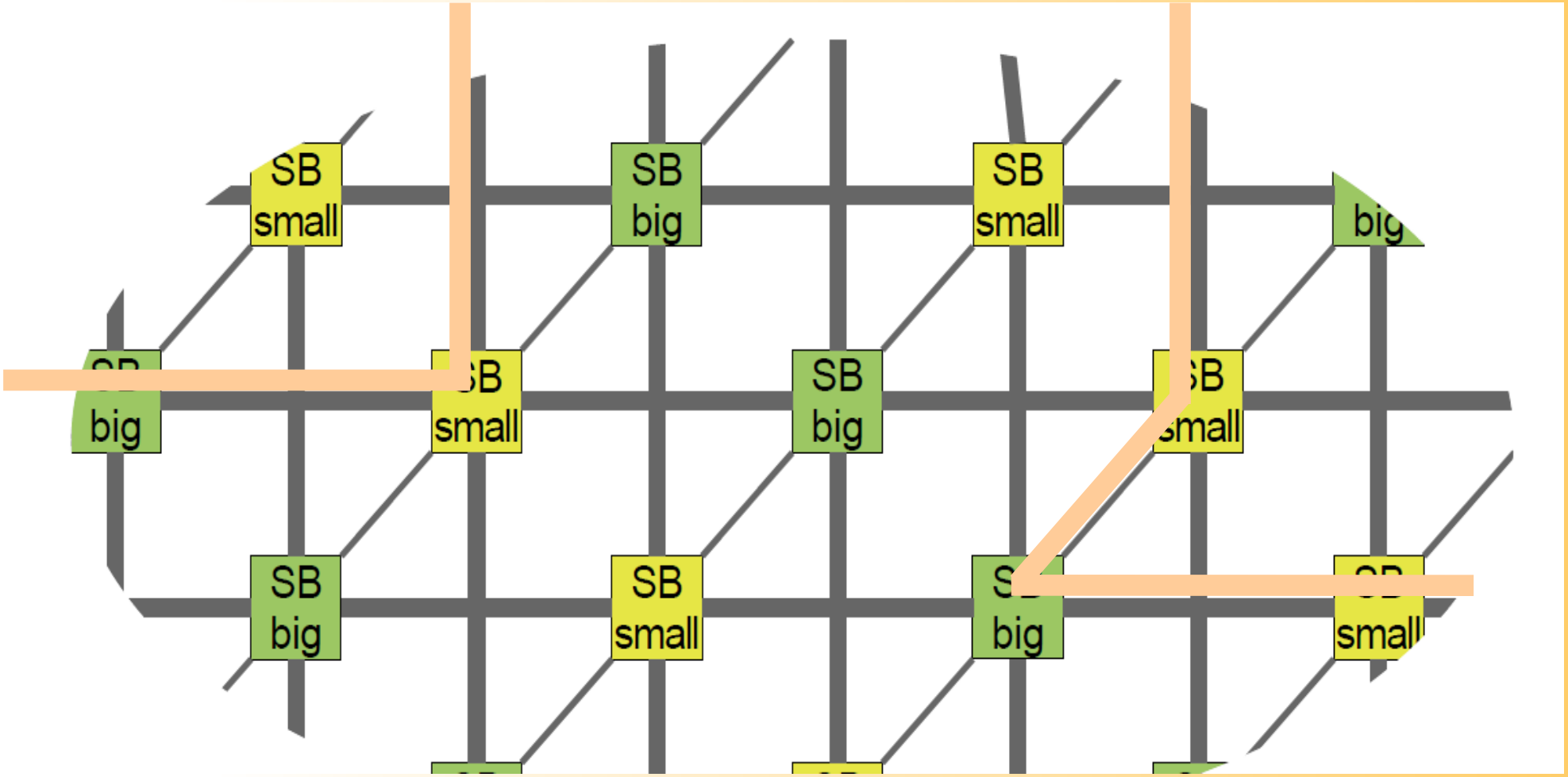


# Interaction of FPGA Circuit Elements

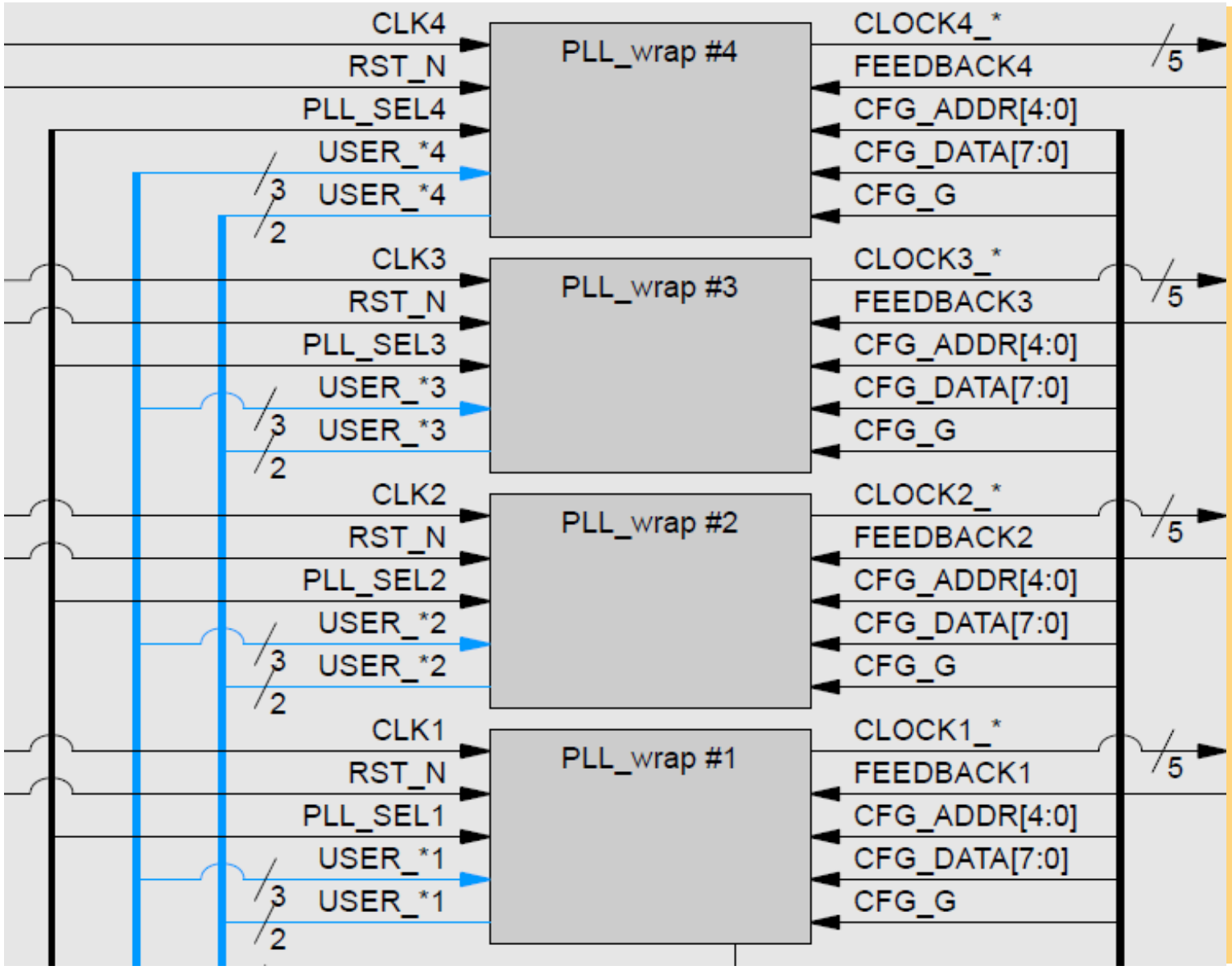


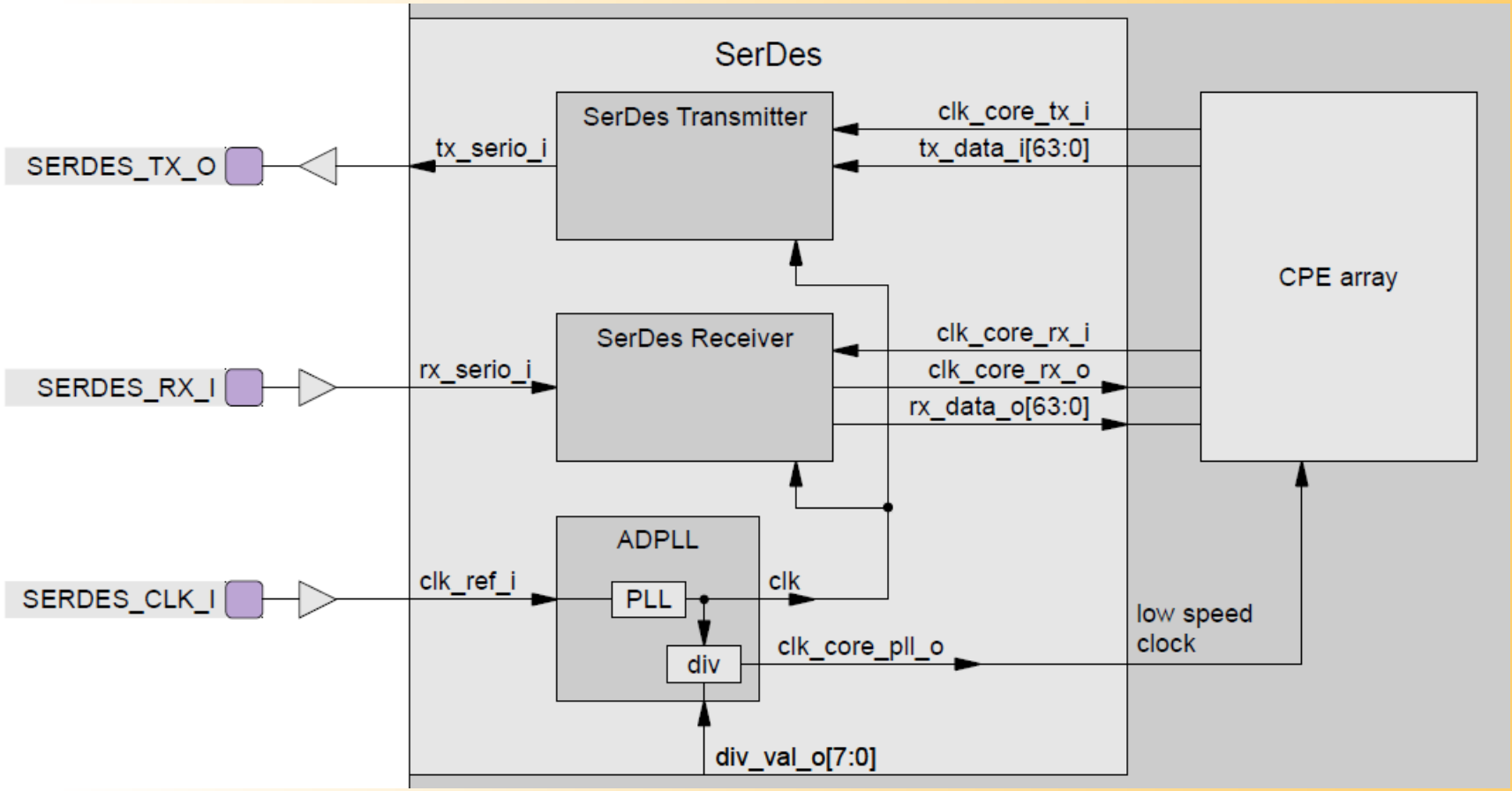
# Direction Change via Switch Boxes



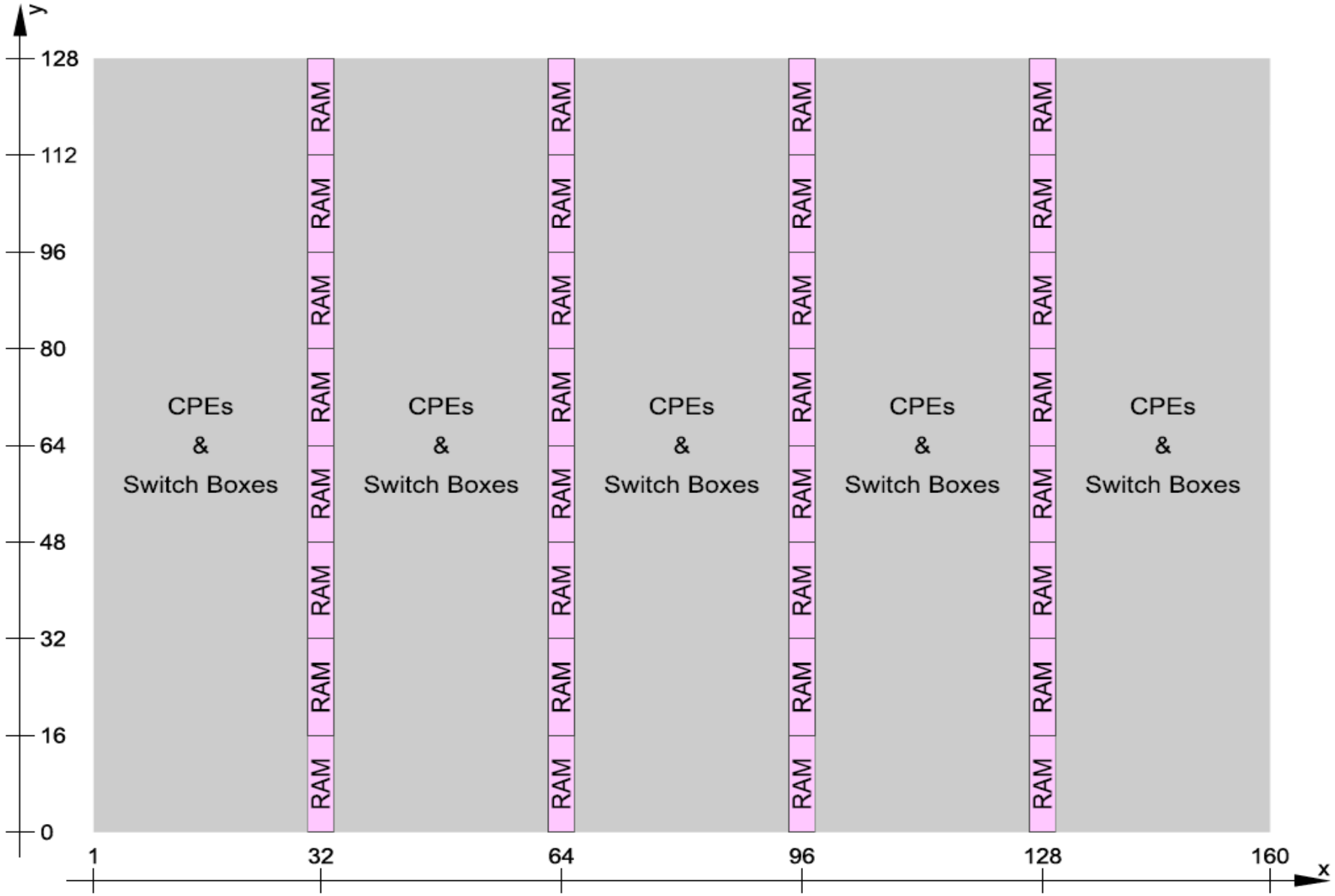
# 4 general purpose PLL circuits



# SERDES high speed interface at 2,5 GBit/s



# Dual Port SRAM map



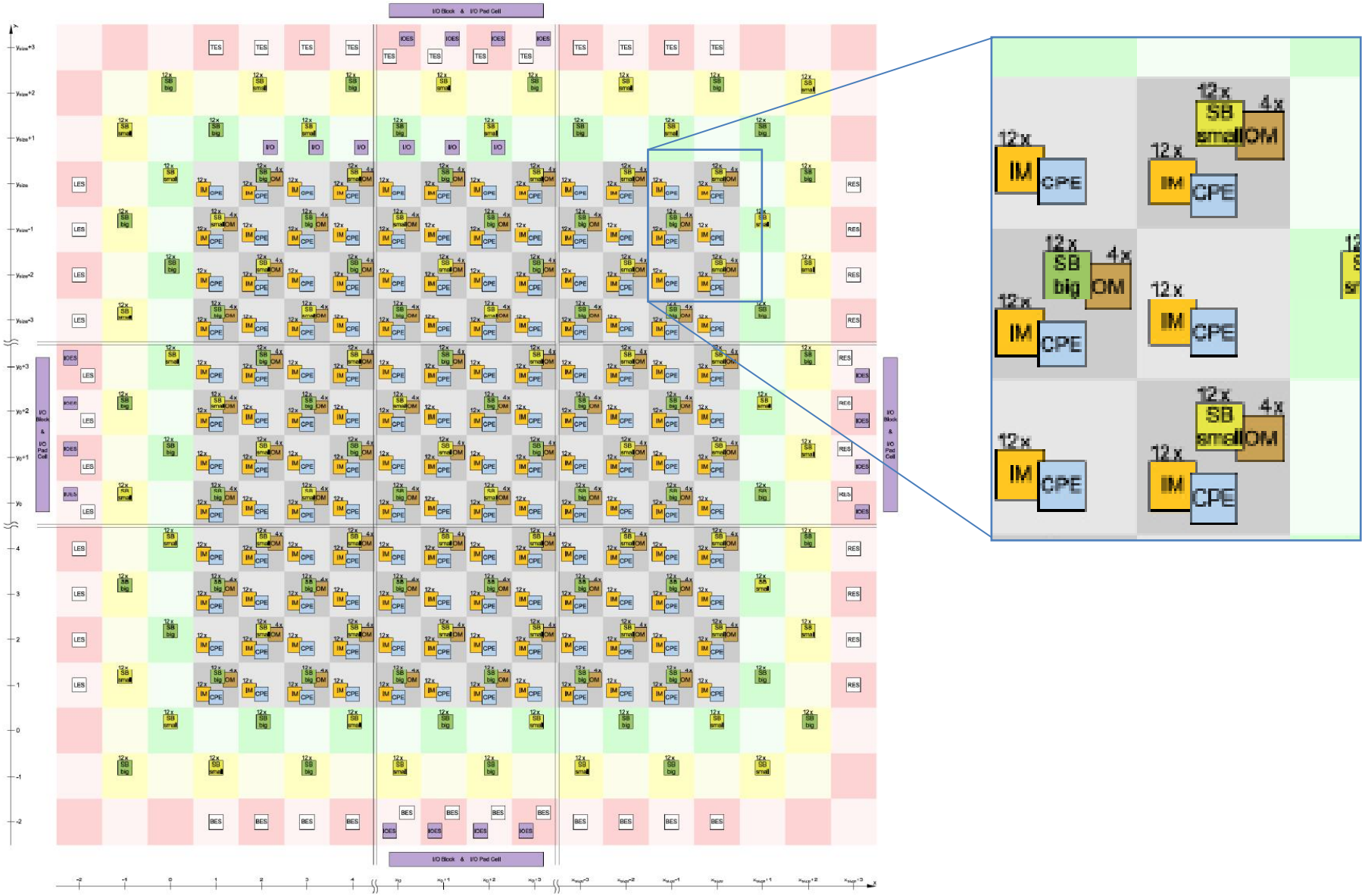
# Dual Port SRAM configuration

| DPSRAM configuration | Non-Split TDP 40 Kbit | Non-Split SDP 40 Kbit |
|---|---|---|
| 32 K × 1 bit | ✓ | ✓ |
| 16 K × 2 bit | ✓ | ✓ |
| 8 K × 5 bit | ✓ | ✓ |
| 4 K × 10 bit | ✓ | ✓ |
| 2 K × 20 bit | ✓ | ✓ |
| 1 K × 40 bit | ✓ | ✓ |
| 512 K × 80 bit | ✗ | ✓ |

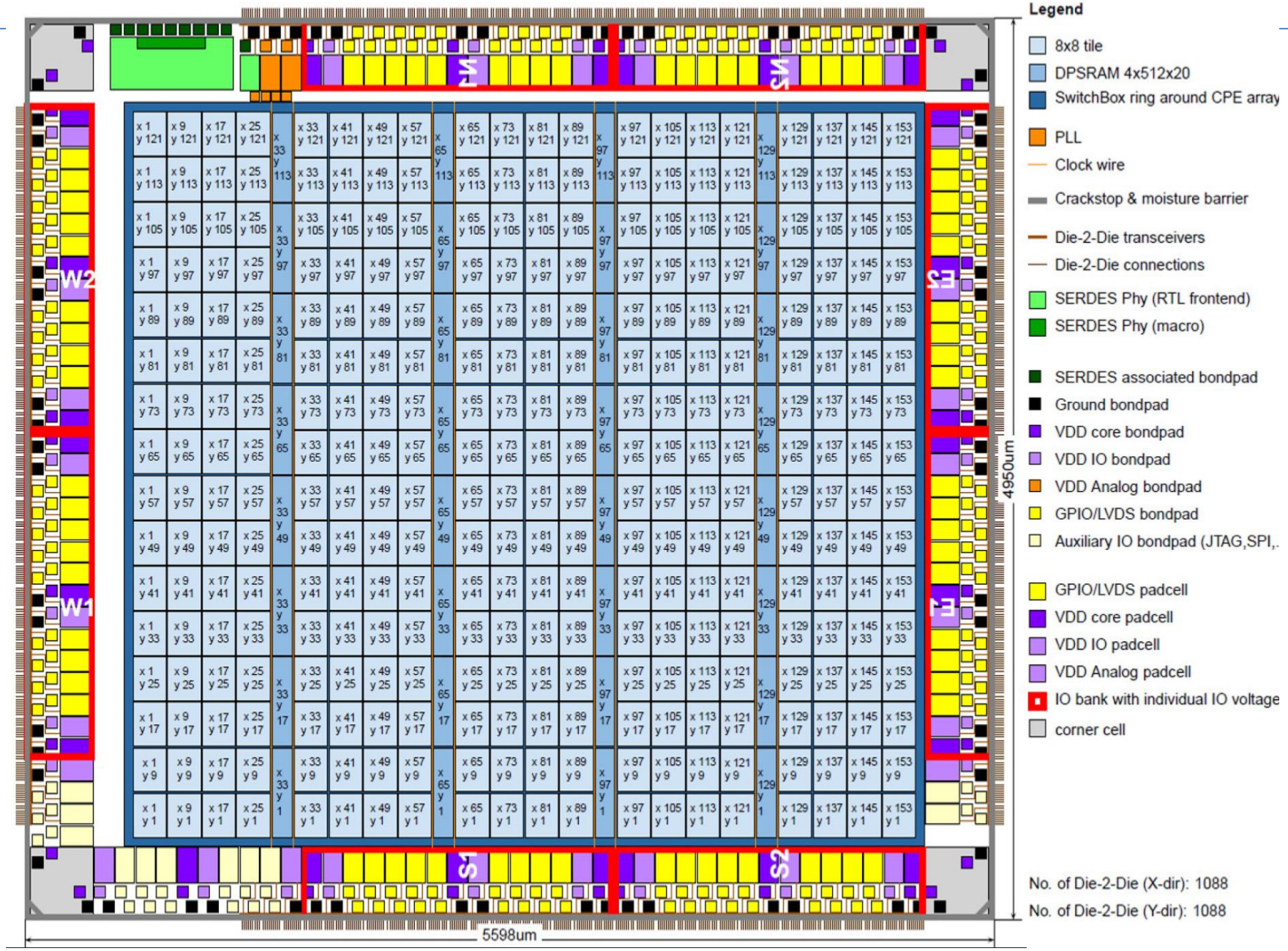
| DPSRAM configuration | Split TDP 2x20 Kbit | Split SDP 2×20 Kbit |
|---|---|---|
| (RAM size per 20 Kbit block) | | |
| 16 K × 1 bit | ✓ | ✓ |
| 8 K × 2 bit | ✓ | ✓ |
| 4 K × 5 bit | ✓ | ✓ |
| 2 K × 10 bit | ✓ | ✓ |
| 1 K × 20 bit | ✓ | ✓ |
| 512 K × 40 bit | ✗ | ✓ |

Every data bit has an own write enable bit

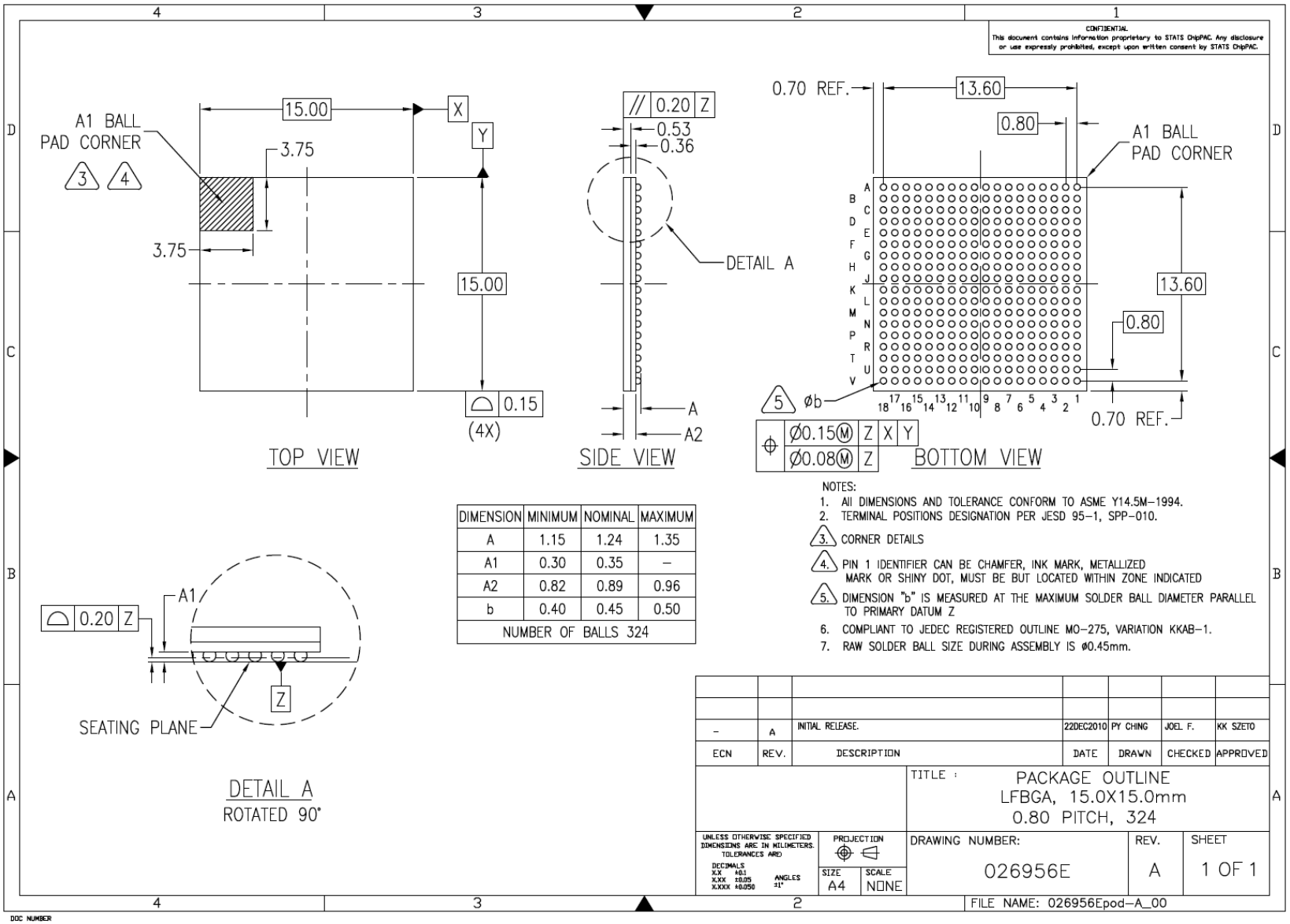
# Overview: Strukture of the FPGA



# Overall View of the FPGA Die



# Package of the FPGA: 324 ball LFBGA



# Package Connections of the FPGA (ball positions and Signal names)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | GND | VDD_WC | IO_NA_A0 | IO_NA_A1 | VDD_NA | IO_NA_A4 | GND | IO_NA_A7 | IO_NB_B0 | GND | IO_NB_B2 | IO_NB_B4 | GND | IO_NB_B7 | IO_EB_B8 | VDD_EB | IO_EB_B5 | GND | A |
| B | IO_WC_A8 | IO_WC_B8 | IO_NA_B0 | IO_NA_B1 | IO_NA_A2 | IO_NA_B4 | VDD_NA | IO_NA_B7 | IO_NB_A0 | VDD_NB | IO_NB_A2 | IO_NB_A4 | VDD_NB | IO_NB_A7 | IO_EB_A8 | GND | IO_EB_A5 | VDD_EB | B |
| C | GND | VDD_WC | IO_WC_A7 | IO_WC_B7 | IO_NA_B2 | IO_NA_A3 | IO_NA_A5 | IO_NA_A6 | IO_NA_A8 | IO_NB_B1 | IO_NB_B3 | IO_NB_B5 | IO_NB_B6 | IO_NB_B8 | IO_EB_B7 | IO_EB_B6 | IO_EB_B4 | IO_EB_A4 | C |
| D | IO_WC_A5 | IO_WC_B5 | IO_WC_A6 | IO_WC_B6 | VDD_WC | IO_NA_B3 | IO_NA_B5 | IO_NA_B6 | IO_NA_B8 | IO_NB_A1 | IO_NB_A3 | IO_NB_A5 | IO_NB_A6 | IO_NB_A8 | IO_EB_A7 | IO_EB_A6 | IO_EB_B2 | IO_EB_A2 | D |
| E | IO_WC_A3 | IO_WC_B3 | IO_WC_A4 | IO_WC_B4 | GND | VDD_NA | GND | VDD_NA | GND | VDD_NB | GND | VDD_NB | GND | VDD_EB | IO_EB_B3 | IO_EB_A3 | VDD_EB | GND | E |
| F | GND | VDD_WC | IO_WC_A2 | IO_WC_B2 | VDD_WC | GND | VDD_NA | GND | VDD | GND | VDD_NB | GND | VDD_EB | GND | IO_EB_B1 | IO_EB_A1 | IO_EB_B0 | IO_EB_A0 | F |
| G | IO_WC_A0 | IO_WC_B0 | IO_WC_A1 | IO_WC_B1 | GND | VDD | GND | VDD | GND | VDD | GND | VDD | GND | VDD_EA | IO_EA_B8 | IO_EA_A8 | IO_EA_B7 | IO_EA_A7 | G |
| H | IO_WB_A7 | IO_WB_B7 | IO_WB_A8 | IO_WB_B8 | VDD_WB | GND | VDD | GND | VDD | GND | VDD | GND | VDD | GND | IO_EA_B6 | IO_EA_A6 | VDD_EA | GND | H |
| J | GND | VDD_WB | IO_WB_A6 | IO_WB_B6 | GND | VDD | GND | VDD | GND | VDD | GND | VDD | GND | VDD_EA | IO_EA_B5 | IO_EA_A5 | IO_EA_B4 | IO_EA_A4 | J |
| K | IO_WB_A5 | IO_WB_B5 | IO_WB_A4 | IO_WB_B4 | VDD_WB | GND | VDD | GND | VDD | GND | VDD | GND | VDD | GND | IO_EA_B3 | IO_EA_A3 | IO_EA_B2 | IO_EA_A2 | K |
| L | IO_WB_A3 | IO_WB_B3 | IO_WB_A2 | IO_WB_B2 | GND | VDD | GND | VDD | GND | VDD | GND | VDD | GND | VDD_EA | IO_EA_B1 | IO_EA_A1 | VDD_EA | GND | L |
| M | GND | VDD_WB | IO_WB_A1 | IO_WB_B1 | VDD_WB | GND | VDD | GND | VDD | GND | VDD | GND | VDD | IO_EA_B0 | IO_EA_A0 | GND | IO_SB_A3 | IO_SB_B3 | M |
| N | IO_WB_A0 | IO_WB_B0 | IO_WA_A8 | IO_WA_B8 | VDD_WA | VDD | GND | VDD | GND | VDD | VDD_SB | GND | VDD_SB | IO_SB_A8 | IO_SB_B8 | N.C. | GND | VDD_SB | N |
| P | IO_WA_A7 | IO_WA_B7 | VDD_WA | GND | VDD_WA | VDD_SA | GND | VDD_SA | GND | VDD_SA | IO_SB_A4 | IO_SB_A7 | IO_SB_B7 | IO_SB_A6 | IO_SB_B6 | VDD_PLL | IO_SB_A2 | IO_SB_B2 | P |
| R | IO_WA_A6 | IO_WA_B6 | IO_WA_A5 | IO_WA_B5 | IO_WA_A0 | IO_SA_A1 | IO_SA_A2 | IO_SA_A4 | IO_SA_A6 | IO_SA_A7 | IO_SB_B4 | GND | IO_SB_A5 | IO_SB_B5 | VDD_SB | GND | IO_SB_A1 | IO_SB_B1 | R |
| T | VDD_WA | IO_WA_A4 | IO_WA_B4 | GND | IO_WA_B0 | IO_SA_B1 | IO_SA_B2 | IO_SA_B4 | IO_SA_B6 | IO_SA_B7 | GND | SER_CLK | SER_CLK_N | VDD_CLK | RST_N | VDD_SER_PLL | GND | VDD_SB | T |
| U | IO_WA_A3 | IO_WA_B3 | VDD_WA | IO_WA_A1 | IO_SA_A0 | VDD_SA | IO_SA_A3 | IO_SA_A5 | VDD_SA | IO_SA_A8 | SER_RX_P | VDD_SER | SER_TX_P | GND | GND | TEST MODE | IO_SB_A0 | IO_SB_B0 | U |
| V | GND | IO_WA_A2 | IO_WA_B2 | IO_WA_B1 | IO_SA_B0 | GND | IO_SA_B3 | IO_SA_B5 | GND | IO_SA_B8 | SER_RX_N | SER_RTERM | SER_TX_N | GND | POR_ADJ | GND | VDD_SER | GND | V |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | |

# Packaged Sample from MPW-Run


**Manufactured by GLOBALFOUNDRIES in Dresden**

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Federal Ministry for Economic Affairs and Energy

on the basis of a decision by the German Bundestag

# Size versions

| | Rel. size | Cologne Programmable Elements | | | Block RAM | | PLLs | SERDES | I/Os | | Package | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | CPEs | 8-Inp-LUT tree | FF/Latches | 20Kb | 40Kb | | | single-ended | differential | balls | size (mm) |
| CCGM1A1 | 1 | 20,480 | 20,480 | 40,960 | 64 | 32 | 4 | 1 | 162 | 81 | 324BGA | 15x15 |
| CCGM1A2 | 2 | 40,960 | 40,960 | 81,920 | 128 | 64 | 8 | 2 | 162 | 81 | 324BGA | 15x15 |
| CCGM1A4 | 4 | 81,920 | 81,920 | 163,840 | 256 | 128 | 16 | 4 | 162 | 81 | 324BGA | 15x15 |
| CCGM1A9 | 9 | 184,320 | 184,320 | 368,640 | 576 | 288 | 36 | 9 | tbd | tbd | 676BGA | 27x27 |
| CCGM1A16 | 16 | 327,680 | 327,680 | 655,360 | 1,024 | 512 | 64 | 16 | tbd | tbd | 676BGA | 27x27 |
| CCGM1A25 | 25 | 512,000 | 512,000 | 1,024,000 | 1,600 | 800 | 100 | 25 | tbd | tbd | 1156BGA | 35x35 |

# Special Features for reduced cost of ownership

## Power

- 3 application modes for the same device only by changing core voltage
  low power, economy, speed

> low inventory because of same device for many projects

- Only 2 supply voltages needed, can be applied in any order
- No excessive start-up currents

> low cost voltage regulators usable

## Package

- Small high ball count packages starting at 15x15mm with 324 balls BGA
- Only 2 signal layers needed on PCB

> low cost conventional PCB

## Supply

- Manufactured in Germany by Globalfoundries

> No unreasonable price rises or tax increase because of trade wars

# Special Features for better performance

## 2x/4y Carry/Propagation lines

- High speed lines without routing Switchboxes.
- could be used also for clock and enable signals
- Is used for adders and multipliers

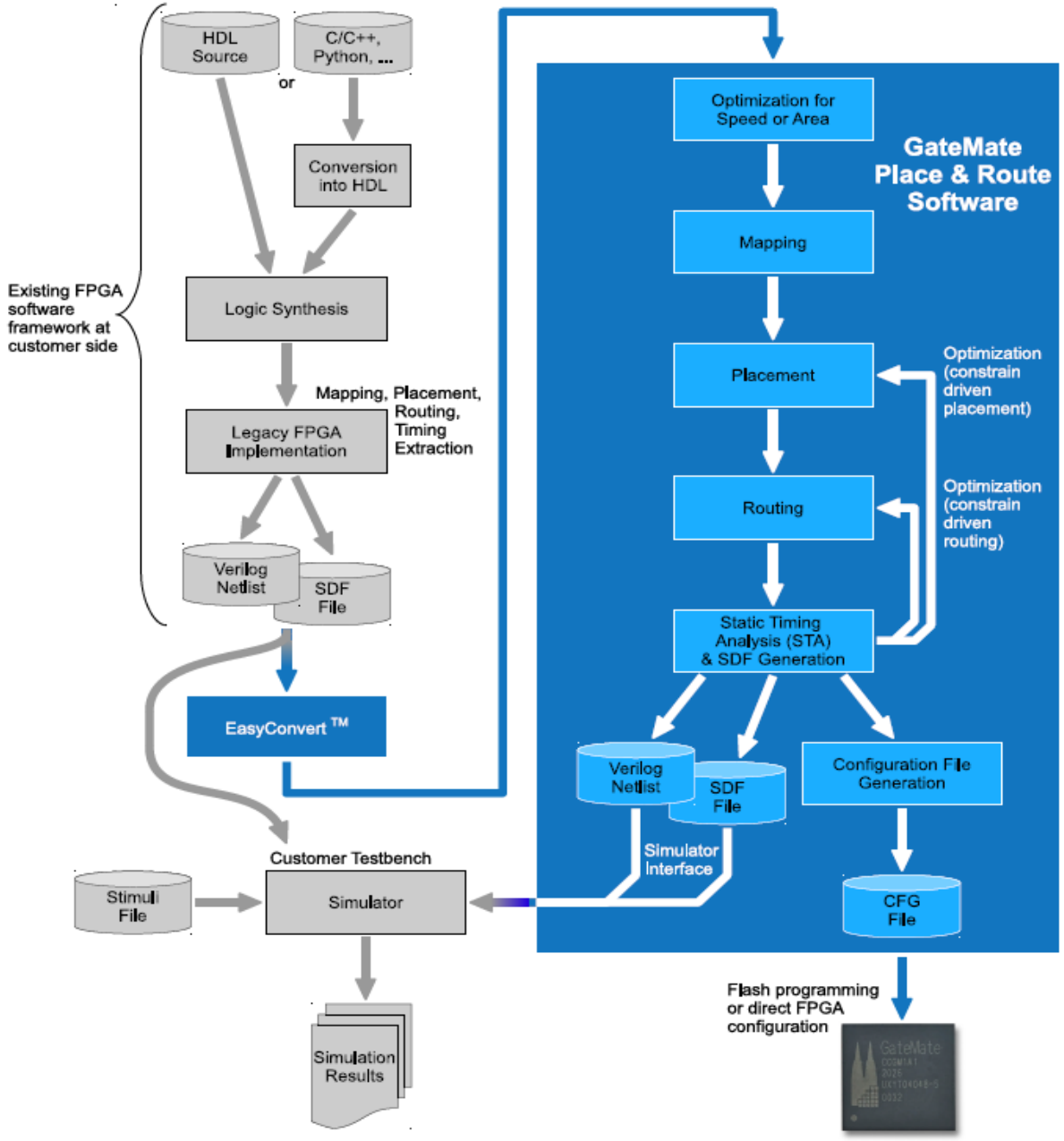
## Very fast configuration from external low cost Flash memory

- 100 MHz quad mode SPI supported
- Low cost general purpose serial Flash device applicable, no need for special PROMs
- Only those configuration latches really used must be configured
- A1 device can be fully configured in only 55ms

## RAM size and orientation

- Superset of known FPGA architectures with 20/40 Bit data width and WE for every bit

# Design flow




**We support Yosys™**

# Thank you for your attention!

Dr.-Ing. Michael Gude

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