GateMate™ FPGA Evaluation Board Datasheet

Generic Evaluation Board for GateMate

DS1003

Datasheet January 2024

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About this Document

This datasheet is the main document in an ensemble of GateMate™ FPGA Evaluation Board documents, which include the following sub-documents:

- **DS1003** – GateMate™ FPGA Evaluation Board Version 3.1 / `CCGM1A1` Schematics
- **DS1003** – GateMate™ FPGA Evaluation Board Version 3.2 / `CCGM1A1` Schematics

All documents of the evaluation board are always updated together. Please make sure that you use these documents with the same date.

For more information please refer to the following documents:

- Technology Brief of GateMate™ FPGA
- **DS1001** – GateMate™ FPGA CCGM1A1 Datasheet
- **DS1002** – GateMate™ FPGA Programmer Board Datasheet
- **UG1002** – GateMate™ FPGA Toolchain Installation User Guide

Cologne Chip provides a comprehensive technical support. Please visit our website for more information or contact our support team.

Revision History

This datasheet is constantly updated. The latest version of the document can be found following the link below:

DS1003 – GateMate™ FPGA Evaluation Board Datasheet

A brief description and download links can be found here:

GateMate™ FPGA Evaluation Board

Date	Remarks
January 2024	Minor changes in Section 2.3 on page 18.
August 2023	• In the course of the release of the PCB version 3.2, the previous datasheet was split into several documents. The main document is valid for all versions. For each version, the schematics, BOM and other board-specific information are available in a separate sub-document. • Some minor changes have been made to board version 3.2, see details in Tables 1.1 and 1.2 on page 14. • Note added regarding a circuitry problem on the evaluation board, see page 27. • Figure 3.11 on page 30 corrected and Figure 3.12 added for new PCB version. • In Table 3.9 on page 37 the signals in the column 'Pmod signal' have been rearranged (only signal names, without changing the electrical circuit).
August 2022	• Figure 3.2 (power supply unit) on page 22 added. • Table 3.8 (GPIO routing details) on page 36 added. • Bill of materials added. • A few small fixes and improvements.
April 2022	Pmod signal assignment added (Table 3.9 on page 37).
March 2022	Initial release.

Chapter 1

Introduction

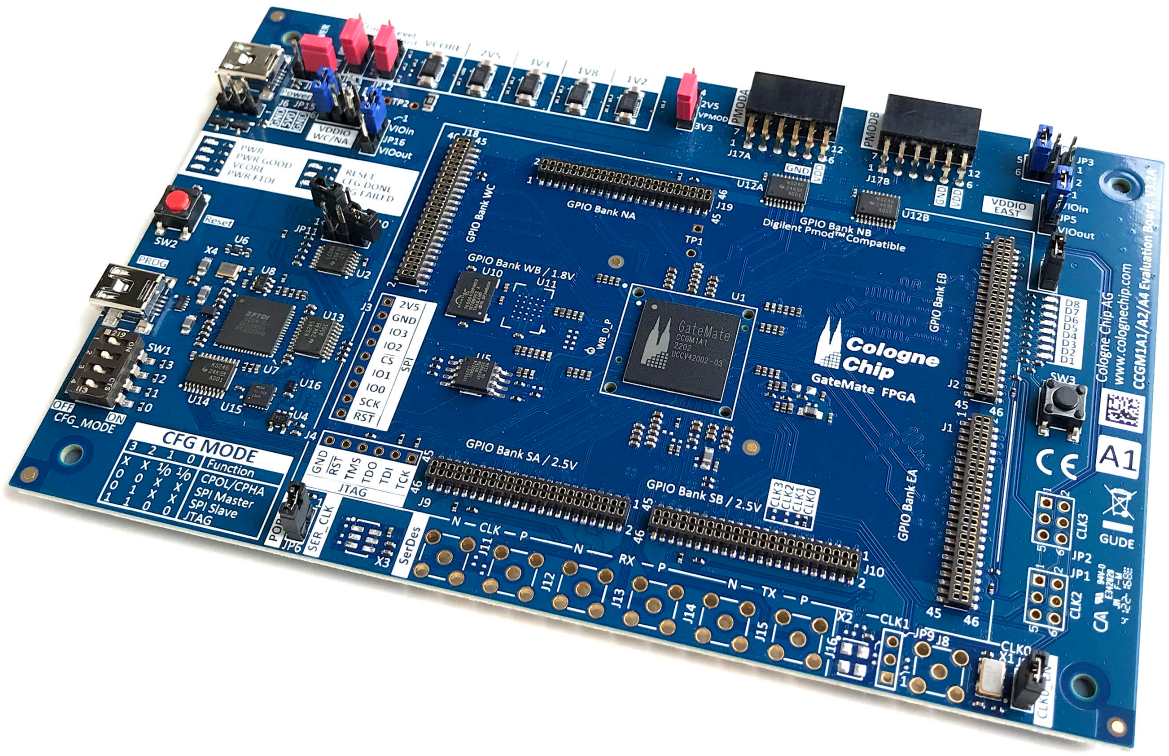

Figure 1.1: *GateMate^{TM} FPGA Evaluation Board Version 3.2A*

The GateMate™ FPGA Evaluation Board is a feature-rich, ready-to-use development platform for the CCGM1A1.

It serves as a reference design and for a direct entry into application development. It is the perfect starting point for all embedded designers as it features

- USB host access,
- JTAG interface,
- SPI interface,
- on-board flash memory,
- serializer / deserializer (SerDes) interface,
- Pmod-compatible interface,
- on-board HyperRAM module,
- 108 accessible general purpose input / outputs (GPIOs),
- 7 status LEDs.

The evaluation kit is available from Cologne Chip. Please visit our website for more information.

Please note!

This datasheet covers the following versions of the GateMate™ FPGA Evaluation Board:

- Version 3.1
- Version 3.2 with minor changes

Differences between these two boards are listed in Tables 1.1 and 1.2 on page 14.

Figure 1.2 gives a brief overview of the evaluation board features. Some GPIO banks have fixed power level according to their function. Others can be configured to different voltages due to the user application requirements.

The printed circuit board (PCB) top view is shown in Figure 1.1. Please note, that some components are prepared for extended features and must be populated by the user, if needed.

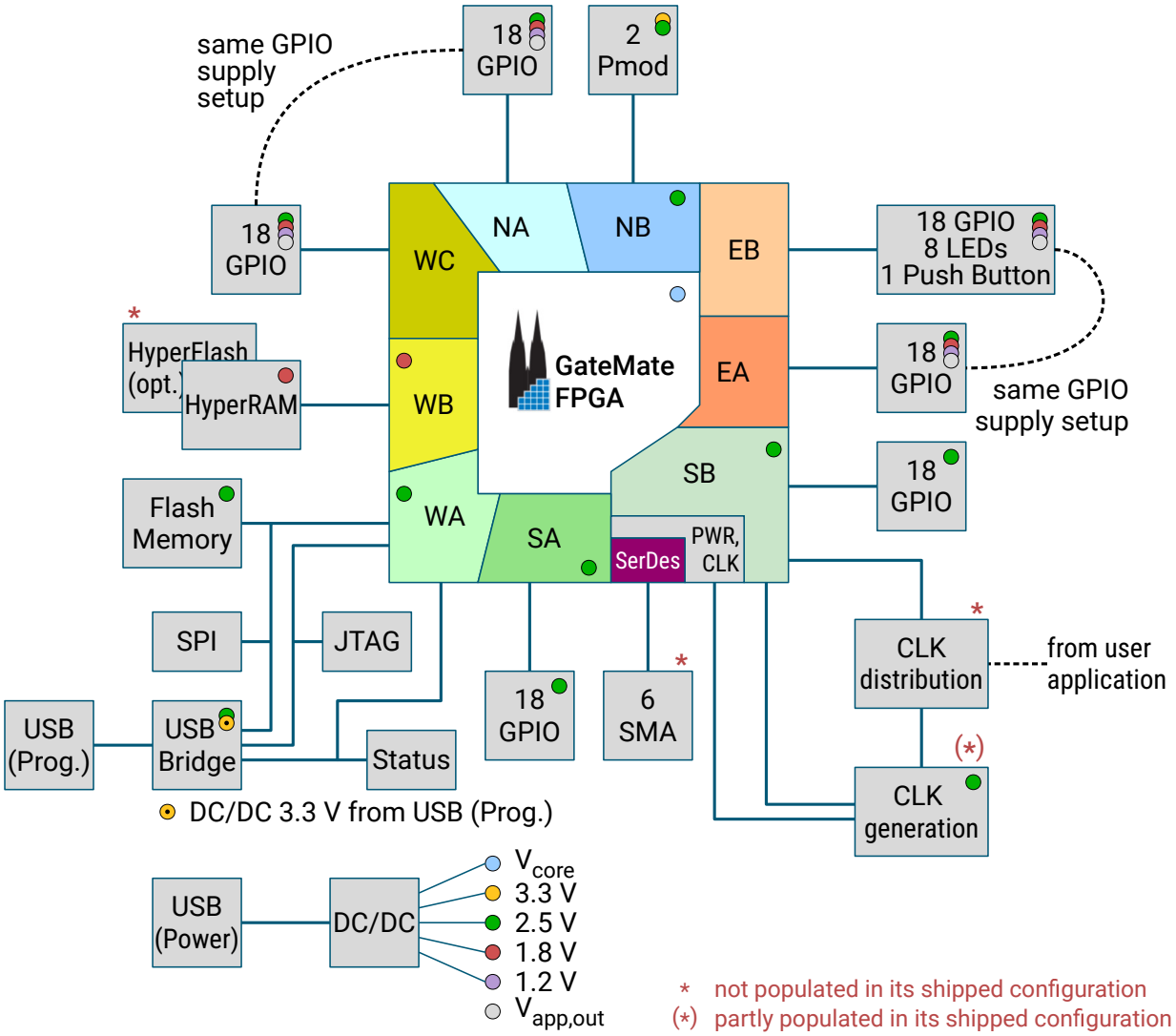

Figure 1.2: *Feature overview of the GateMate™ FPGA Evaluation Board*

Table 1.1: *Changes of signal names between evaluation board versions 3.1 and 3.2*

Schematic Page	Title / Module	Version 3.1	Version 3.2
3	GPIO Module	CFG_FAILED_APP	/CFG_FAILED_APP
8	Configuration GPIO Module	CFG_FAILED (net) CFG_FAILED (port)	/CFG_FAILED /CFG_FAILED_APP
9	SPI / JTAG Interface	CFG_FAILED /FAILED –	/CFG_FAILED FAILED DONE (port added)
10	Programmer Wrapper	/FAILED CFG_FAILED	FAILED /CFG_FAILED
11	Programmer	/FAILED_A /FAILED_B	FAILED_A FAILED_B

see schematics in GateMate™ FPGA Evaluation Board Version 3.1 / CCGM1A1 Schematics
GateMate™ FPGA Evaluation Board Version 3.2 / CCGM1A1 Schematics

Table 1.2: *Differences between evaluation board versions 3.1 and 3.2*

Schematic Page	Title / Module	Ver.	Changes
8	Configuration GPIO	3.2	U3 (NL27WZ04) and C14 (100n) removed
		3.2	CFG_DONE signaling D10 and R28 moved to other side of SPI / JTAG interface module
10	Programmer Wrapper	3.2	Module port DONE added
		3.2	Flip-flop added between signals CFG_DONE and DONE
		3.1 3.2	U15 is SN74AUP2G00DCUR (dual NAND gate) U15 is SN74AUC00RGYR (quad NAND gate)
		3.2	U16 (SN74AUP1G04DRYR) and C14 (100n) added
		3.1 3.2	U13.A6 is connected to CFG_DONE U13.A6 is connected to DONE
		3.1 3.2	U14.A6 is connected to CFG_DONE U14.A6 is connected to DONE
20	Power Supply	3.2	R89 . . R94 values changed

see schematics in GateMate™ FPGA Evaluation Board Version 3.1 / CCGM1A1 Schematics
GateMate™ FPGA Evaluation Board Version 3.2 / CCGM1A1 Schematics

Chapter 2

Startup

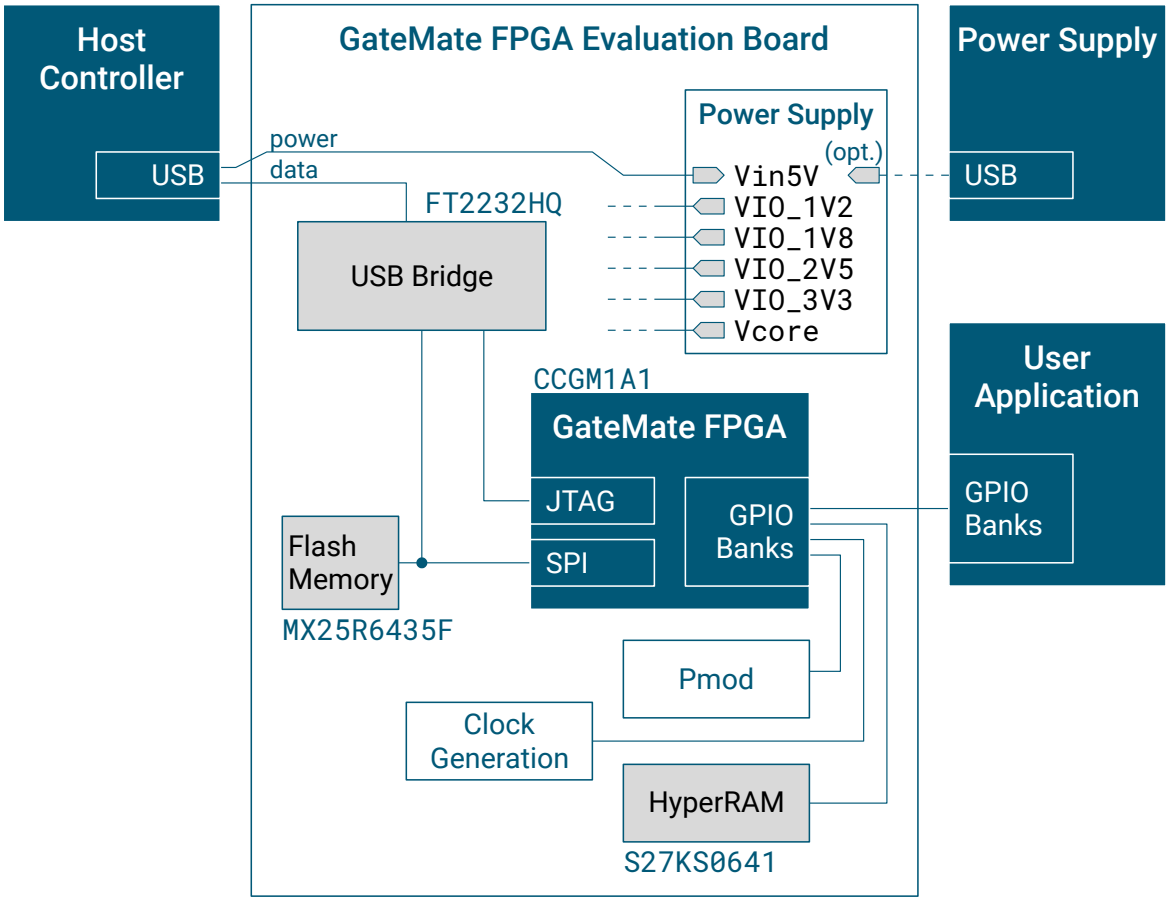

Figure 2.1: *Block diagram of the GateMate™ FPGA Evaluation Board*

2.1 Block Diagram

The GateMate™ FPGA Evaluation Board offers a quick access to the CCGM1A1 functions. Figure 2.1 gives a simplified overview of the printed circuit board (PCB) block diagram. A single supply voltage from any USB supply is typically used for powering the PCB and the user application.

The FPGA configuration can be loaded in two different ways. The on-board flash memory can automatically set up the FPGA configuration after reset. Alternatively, a host controller can be used to load the FPGA configuration. These functions and additional features on the SPI und JTAG interface are described in Chapter 3.3 from page 27.

The user application connects the general purpose input / output (GPIO) banks of the GateMate™ FPGA and some additional signals like reset and clock to fulfill further application requirements.

2.2 Connection to the User Application

The interface to the GPIO banks is implemented with 2-row 46-pin through-hole connectors with pin pitch 1.27 mm. The user application can use standard male pin header 2×23 to connect the GPIO banks and some further signals.

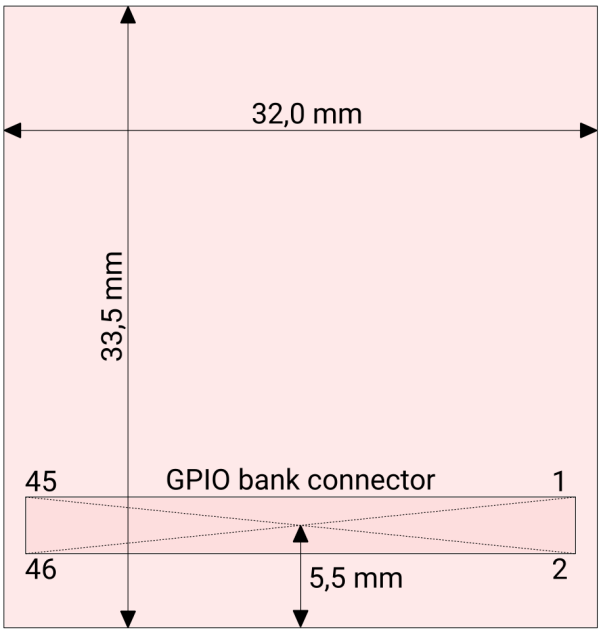

Figure 2.2: *Recommended maximum dimensions of a user application PCB for a single GPIO bank and horizontal assembly (top view)*

Due to through-hole technology, the user application can either be connected at the top side of the evaluation board, or it can be mounted below. It is usually advisable to assemble the user application on the top side for an easy access to the user circuitry. Then,

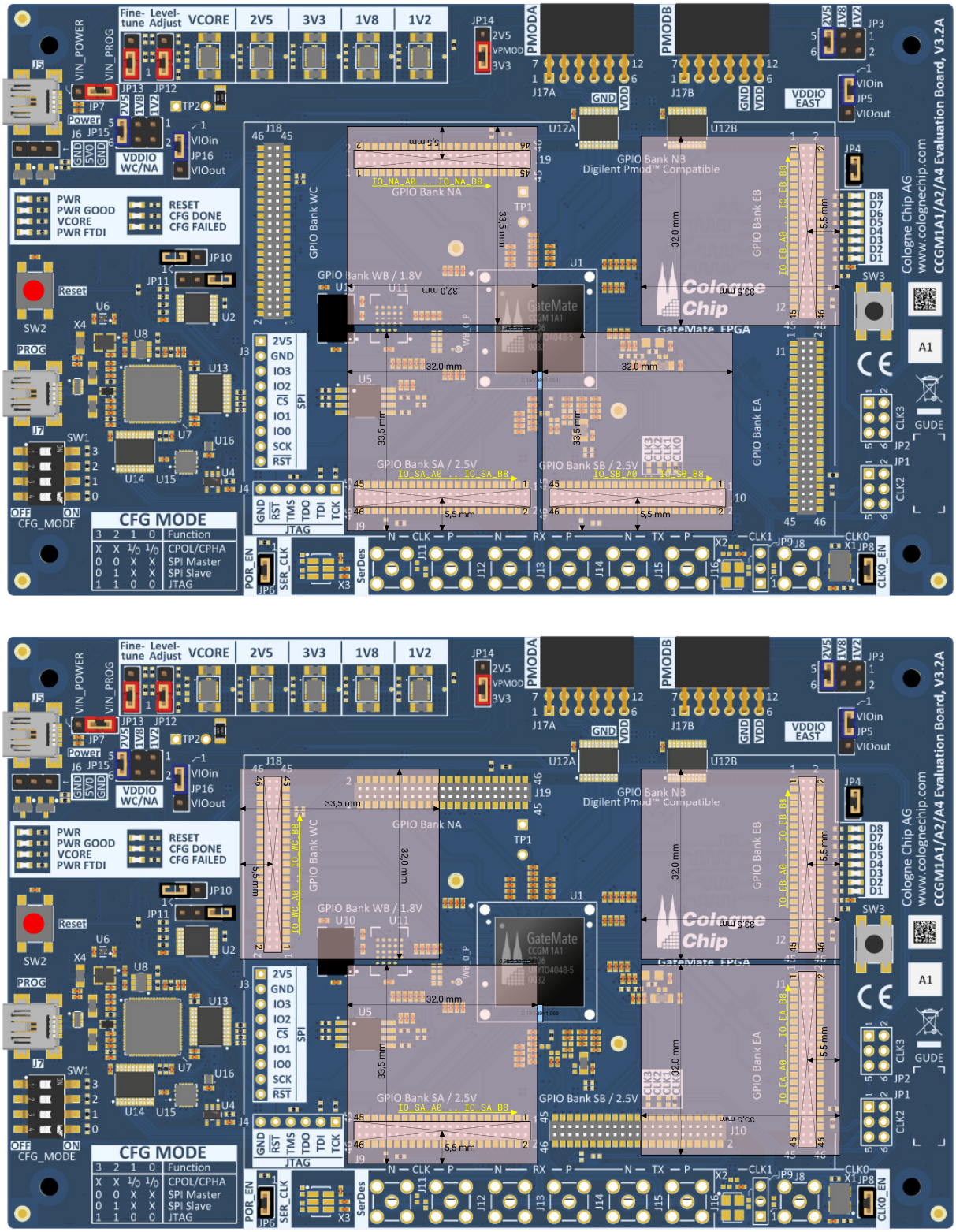

Figure 2.3: *Examples of assembling several 1-bank user applications at the same time*

it should be noted that all tall components are outside the rectangular area of the GPIO bank connectors.

For a user application with access to a single GPIO bank, e.g., the maximum PCB dimensions should not exceed 32.0×33.5 mm for horizontal assembly. Furthermore, the location of the GPIO pin header should be as shown in Figure 2.2. With this arrangement,

a) the user PCB can be plugged onto every GPIO bank and
b) several user PCBs can be used at the same time as shown in Figure 2.3.

When assembling the user PCB below the evaluation board there are no restrictions due to tall components.

When assembling the user PCB upright, there are no restrictions concerning the user PCB length. However, the specified width of 32.0 mm should not be exceeded.

For the design of user applications with more than one GPIO bank please see the evaluation board dimensions in documents GateMate™ FPGA Evaluation Board Version 3.1 and Version 3.2 Schematics, here in both cases Figure 1.1 on page 8.

2.3 Connection to the Host Controller

The GateMate™ FPGA Evaluation Board requires a computer with Linux or Windows operating system as follows:

- Supported Linux environments:
  - Debian-based Linux (Debian, Ubuntu, ...) with `apt` package manager
  - Arch-based Linux (Arch, Manjaro, ...) with `pacman` package manager
  - Red Hat-based Linux (Fedora, ...) with `dnf` or `yum` package manager
- Windows environments:
  - Windows 7 or later, 64 bit
  - Zadig USB driver installer (`https://zadig.akeo.ie/`)

When first plugged into the computer's USB port, drivers should load by default.

In Windows environments, it is necessary to install USB drivers using Zadig. Download the software and connect the GateMate™ FPGA Evaluation Board to your USB port. In the Zadig Window, select **Options > List All Devices** to refresh the device list. Then, unmark **Options > Ignore Hubs or Composite Parents**. From the drop-down list, select **GateMate™ FPGA Evaluation Board 3.2A (Composite Parent)**. Now select **libusb-win32 (any version)** from the driver list and replace the drivers (see Figure 2.4).

Replacing drivers might take a moment. Your GateMate™ FPGA Evaluation Board should then be listed as **libusb-win32 device**s in the Device Manager as shown in Figure 2.5.

In Linux environments, drivers are automatically loaded correctly.

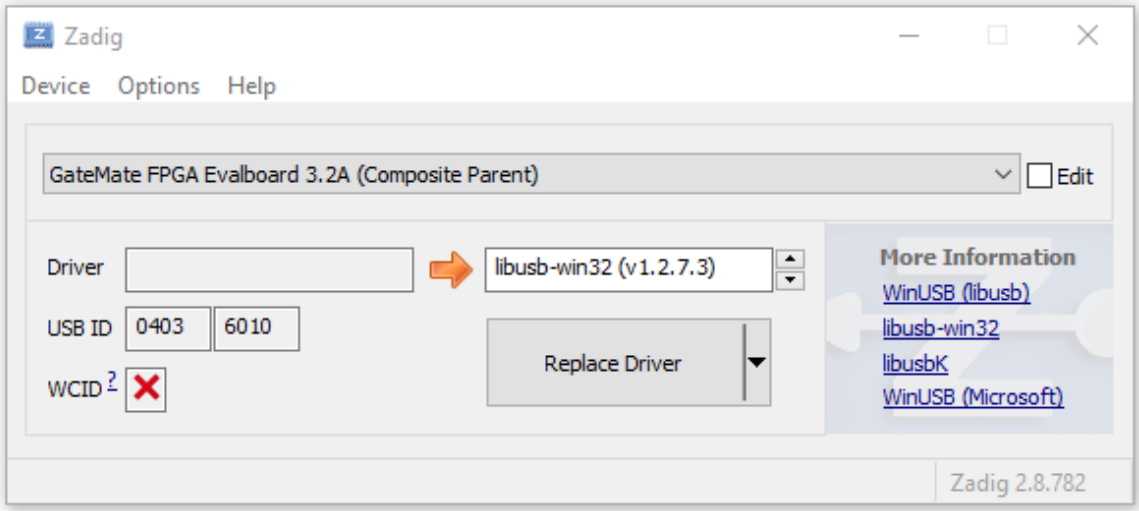

Figure 2.4: *Zadig Window with selected GateMate™ FPGA Evaluation Board*

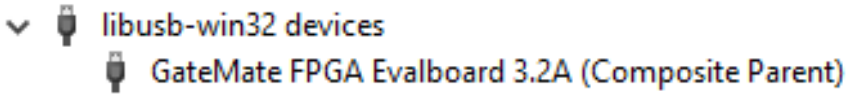

Figure 2.5: *GateMate™ FPGA Evaluation Board in Device Manager*

The tool setup for the Cologne Chip GateMate™ series is described in **UG1002** – GateMate™ FPGA Toolchain Installation User Guide

Chapter 3

GateMate™ FPGA Evaluation Board Functions

3.1 PCB Power Supply

The power supply unit consists of five DC-DC converters MPM3833C which offer all voltages to fulfill the requirements of a wide range of user applications. All converters are feed from a single source. Typically an USB supply can be used.

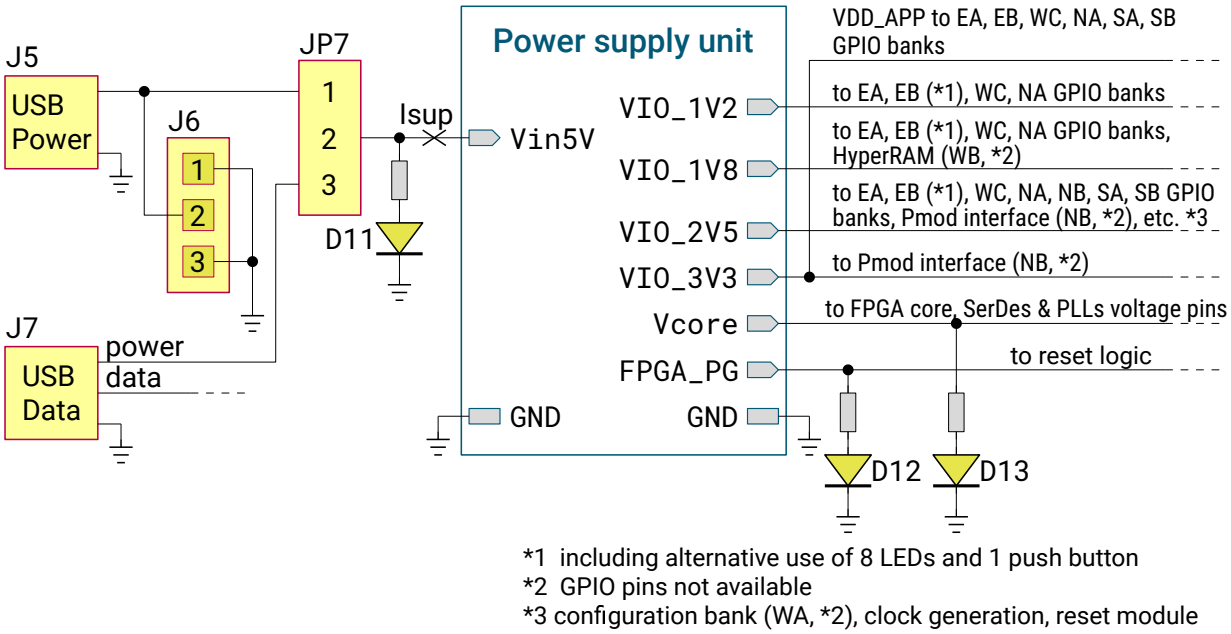

Figure 3.1: *PCB power supply*

Figure 3.1 shows that power supply can either be feed in from the USB connector J5 or it can be taken from the USB data connector J7 instead. Please ensure, that enough power can be delivered from the USB host.

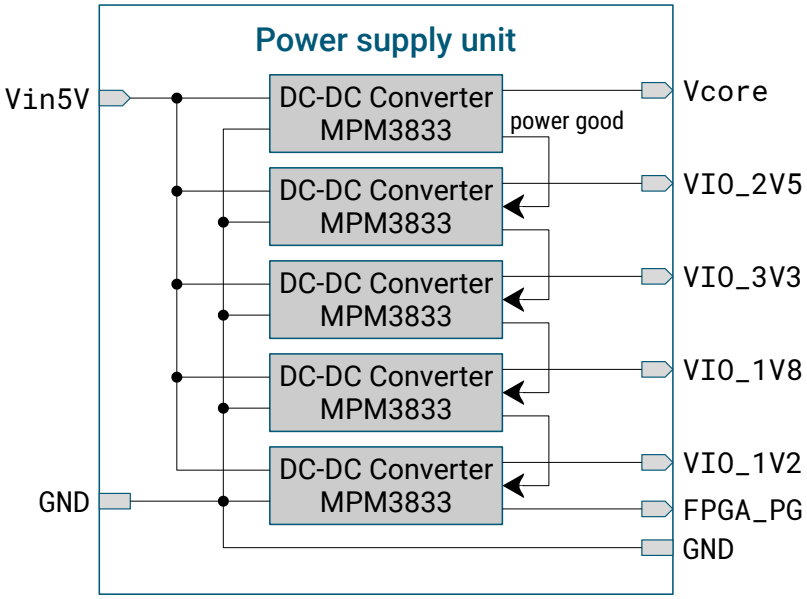

Figure 3.2: *DC-DC converter chain*

Alternatively, power supply can be feed from any other source via connector J6. The required input voltage is 4.0 . . 6.0 V.

All DC-DC converters are chained with their power good signal as shown in Figure 3.2. At the end of the chain, signal FPGA_PG is feed to the reset circuitry (see Figure 3.10 on page 30). The FPGA can only go into operation when all converters provide a stable output voltage.

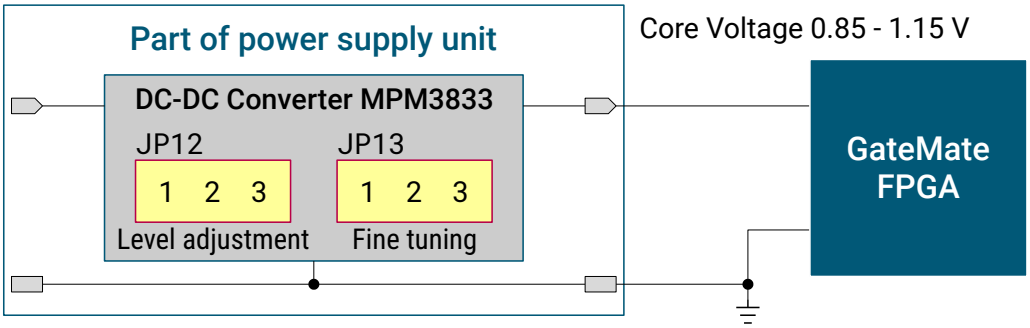

Figure 3.3: *GateMate™ FPGA core voltage*

The DC-DC converters have a fixed output voltage. Only the DC-DC converter for the FPGA core voltage can be adjusted as shown in the block diagram in Figure 3.3.

The FPGA core voltage can be set up to different levels for low power mode, economy mode or speed mode. Furthermore, typical voltage can be chosen as well as minimum and maximum levels. Jumper settings are described in Table 3.1.

Table 3.1: *JP12 and JP13 jumper settings for FPGA core voltage*

JP12	JP13	Core Voltage	Function
open	open	0.85 V	low power mode, min
open	1 - 2	0.90 V	low power mode, typical
open	2 - 3	0.95 V	low power mode, max
1 - 2	open	0.95 V	economy mode, min
1 - 2	1 - 2	1.00 V	economy mode, typical
1 - 2	2 - 3	1.05 V	economy mode, max
2 - 3	open	1.05 V	speed mode, min
2 - 3	1 - 2	1.10 V	speed mode, typical
2 - 3	2 - 3	1.15 V	speed mode, max

Important note:

Please ensure to disconnect the power supply before changing the jumper settings to avoid damage of the devices.

3.2 GPIO Power Supply

The CCGM1A1 FPGA offers nine general purpose input / output (GPIO) banks. Their GPIO supply voltage is set up in different ways on the evaluation board as shown in Table 3.2.

Table 3.2: *Assignment of GPIO power supply scheme to GPIO banks*

Figure	Page	GPIO banks	Scheme characteristics
3.4	24	WC, NA, EA	GPIO voltage selected from three on-board sources or the application voltage
3.5	25	EB	GPIO voltage selected from three on-board sources or the application voltage, additional functions (LEDs and user button)
3.6	26	SA, SB	Single 2.5 V voltage supply
–	–	WA	Configuration bank, 2.5 V supply
3.18	38	WB	HyperBus memory, 1.8 V supply
3.17	37	NB	Pmod interface, 2.5 V supply

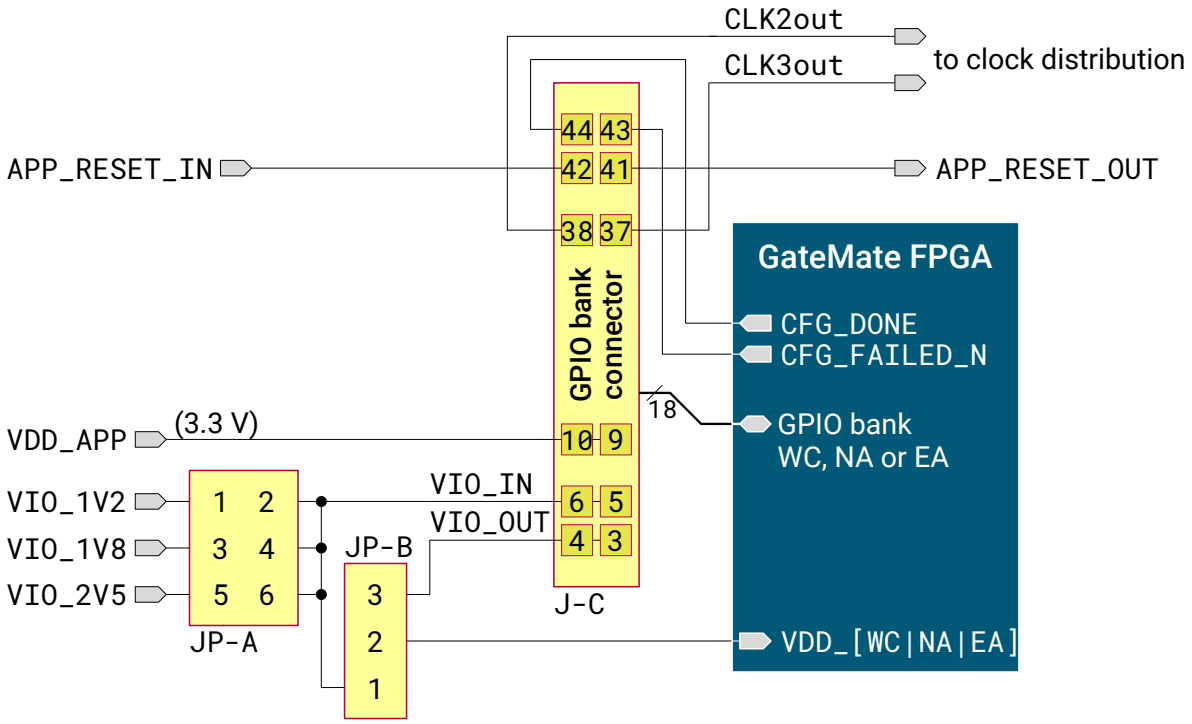

Figure 3.4: *GPIO supply with voltage selection*

Figure 3.4 shows the configurable GPIO supply setup for GPIO banks `WC`, `NA` and `EA`. These banks can select one of three on-board voltages as well as `VIO_OUT` feed from the user application. The selected on-board voltage is also feed to the user application (`VIO_IN`) and can be used to supplement the separat `VDD_APP` voltage.

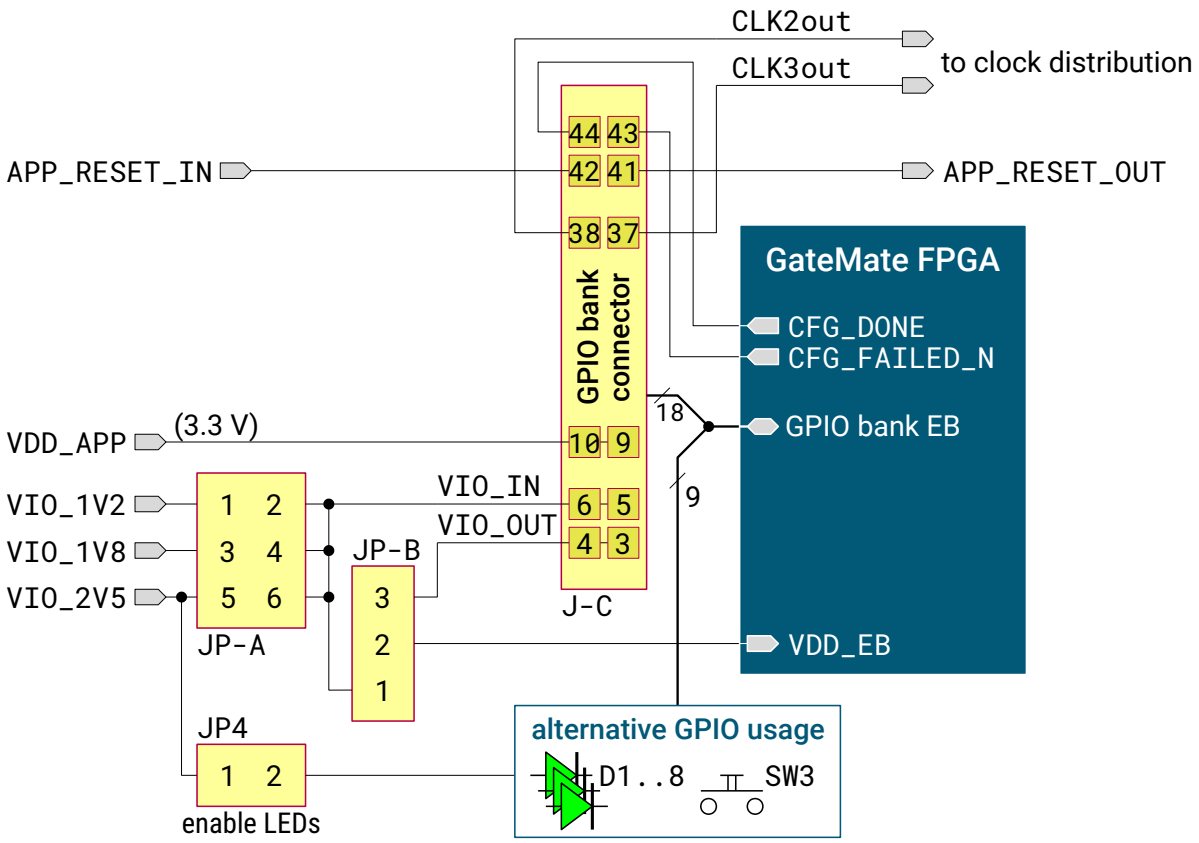

Figure 3.5: *GPIO supply with voltage selection and alternative LEDs and push button*

The same GPIO supply scheme is available for GPIO bank EB but additional functionality is implemented for some GPIO signals as shown in Figure 3.5 and Table 3.3. Eight LEDs can be enabled with Jumper JP4 set. With open jumper, the normal GPIO function is available at connector J-C (J2). Switch SW3 has an on-board pull-up resistor, which should be

Table 3.3: *Additional functions on GPIO bank EB*

Component	GPIO	Funktion
D1	IO_EB_B1	low: on (green), high: off
D2	IO_EB_B2	ditto
D3	IO_EB_B3	ditto
D4	IO_EB_B4	ditto
D5	IO_EB_B5	ditto
D6	IO_EB_B6	ditto
D7	IO_EB_B7	ditto
D8	IO_EB_B8	ditto
SW3	IO_EB_B0	pressed: low, unpressed: high

Table 3.4: *Jumper JP-A, JP-B and connector J-C designators*

Figure	JP-A	JP-B	J-C	GPIO bank
3.4 (page 24)	JP15	JP16	J18	WC
	JP15	JP16	J19	NA
	JP3	JP5	J1	EA
3.5 (page 25)	JP3	JP5	J2	EB
3.6 (page 26)	–	–	J9	SA
	–	–	J10	SB

taken into account when using the normal GPIO function instead. Table 3.3 shows the additional EB GPIO functions in detail.

Table 3.4 gives an overview of jumpers JP-A and JP-B and connector J-C availability for the individual GPIO banks.

Finally, GPIO banks SA and SB have a fixed supply voltage 2.5 V (see Figure 3.6). Again, the user application supply is both, VDD_APP and the GPIO voltage VIO_2V5.

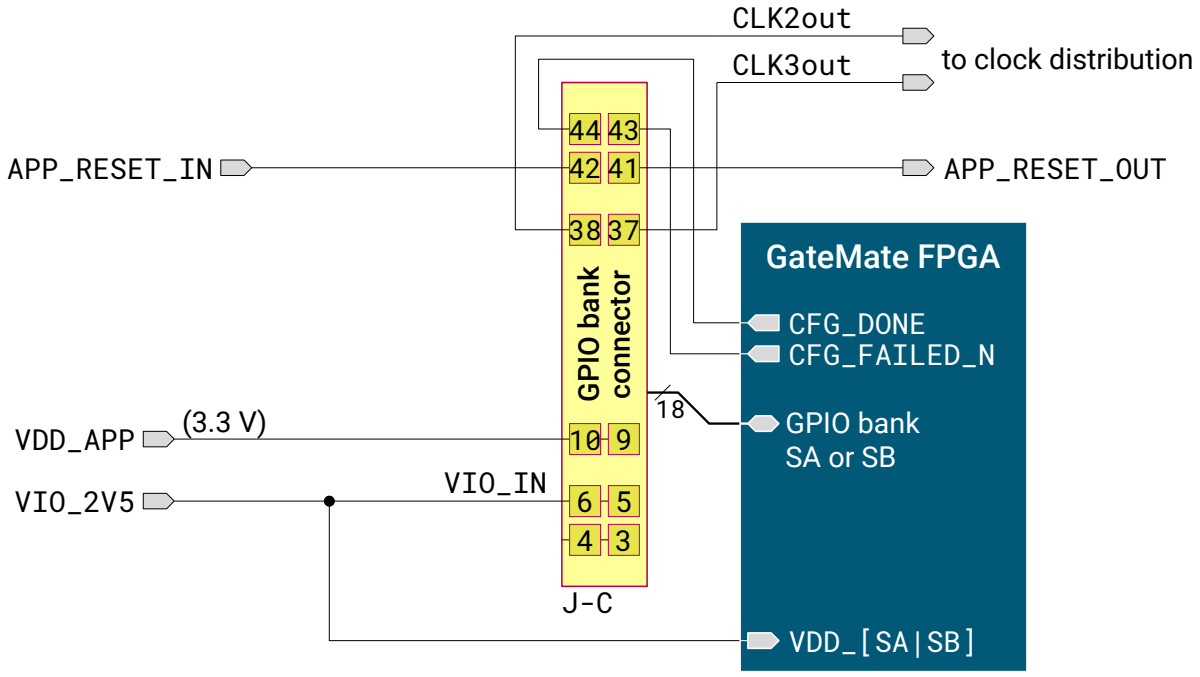

Figure 3.6: *GPIO supply with single voltage*

3.3 SPI and JTAG Data Busses

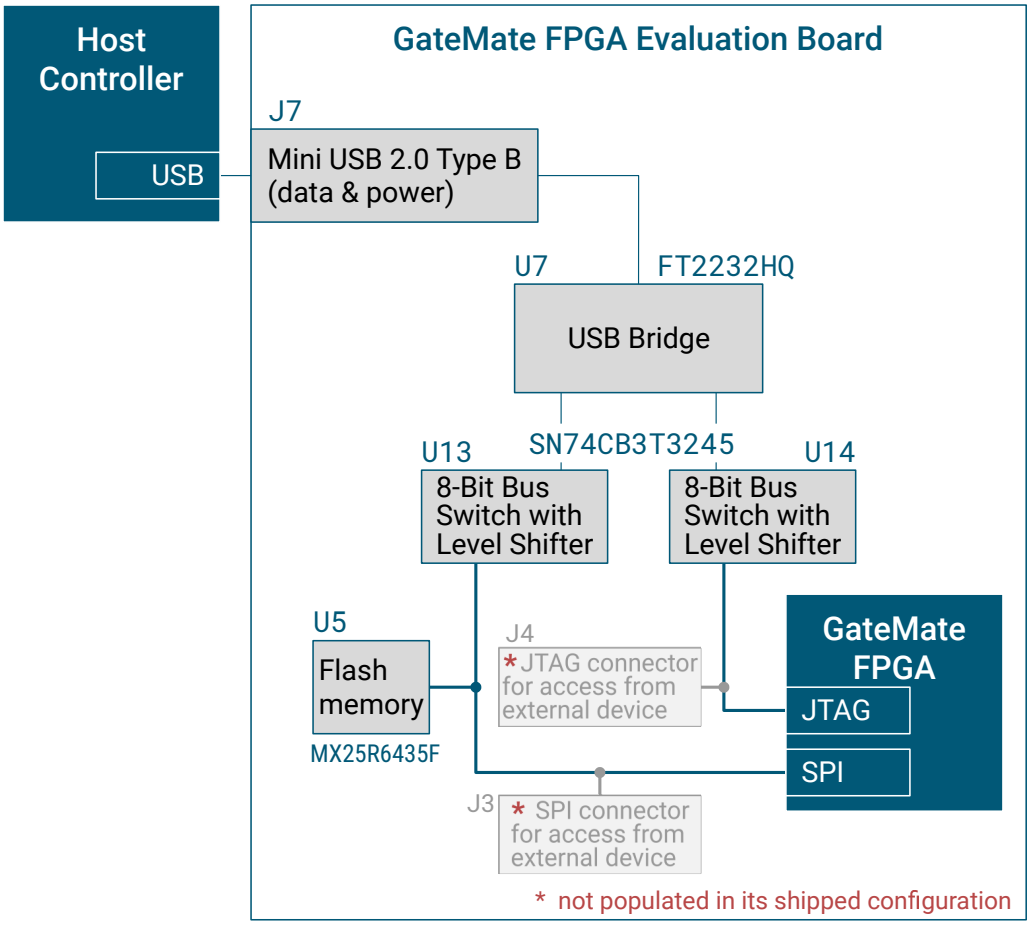

Figure 3.7: *Block diagram with details of SPI and JTAG interfaces*

The SPI bus can be accessed from any user device. For this, connector J3 (2.54 mm pin pitch, 9 pins) has to be populated. Figure 3.8 shows the pin assignment of the SPI connector.

The JTAG interface can be accessed from any user device. For this, connector J4 (2.54 mm pin pitch, 6 pins) has to be populated. Figure 3.9 shows the pin assignment of the JTAG connector.

> **Please note!**
>
> If the USB bridge U7 is switched off (USB cable not connected or suspend mode), both the level shifter U13 and the FPGA U1 drive on the SPI bus at the same time. Because of the series resistors R38 . . R41 there is no short circuit here.
>
> However, this circuitry error only leads to a problem if the flash drives less strongly than the level shifter. This depends on the types of the used devices. On the evaluation board the circuitry works, but it is not recommended to use it in product designs!

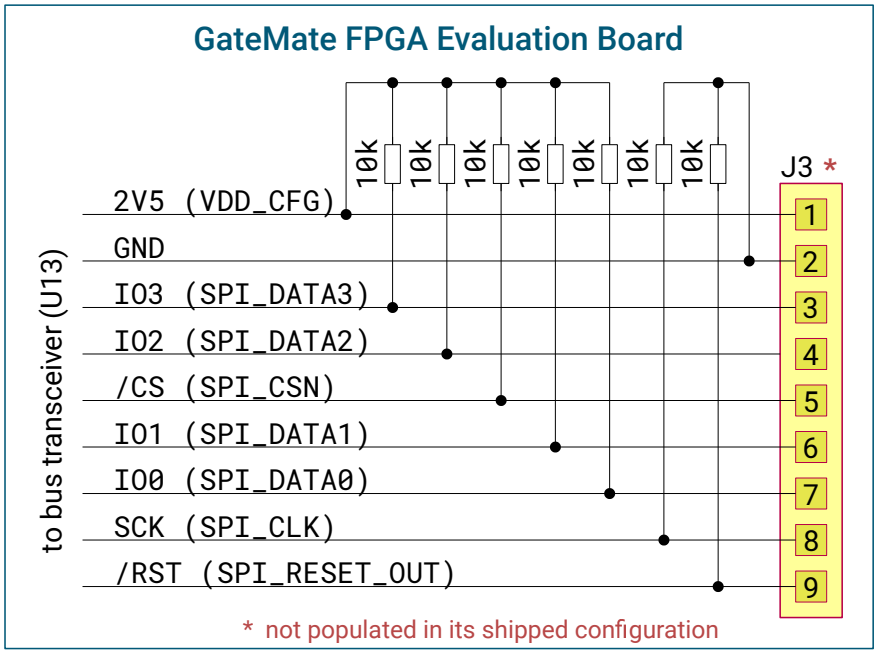

Figure 3.8: *Optional SPI interface connector J3*

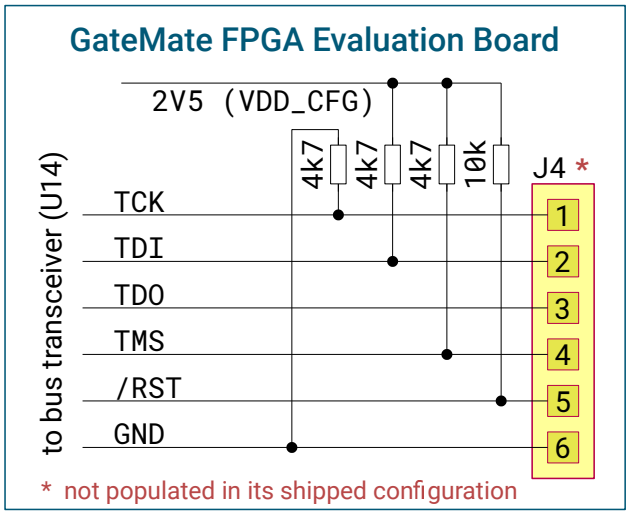

Figure 3.9: *Optional JTAG interface connector J4*

3.4 Configuration Mode and Reset

There are several ways to load the FPGA configuration. The configuration mode is choosen with switch SW1 setup as shown in Table 3.5.

Table 3.5: *GateMate^{TM} FPGA configuration modes*

CFG_MD[3:0] *		Configuration mode	
0x0	0b0000	SPI Master Mode	CPOL = 0, CPHA = 0
0x1	0b0001	SPI Master Mode	CPOL = 0, CPHA = 1
0x2	0b0010	SPI Master Mode	CPOL = 1, CPHA = 0
0x3	0b0011	SPI Master Mode	CPOL = 1, CPHA = 1
0x4	0b0100	SPI Slave Mode	CPOL = 0, CPHA = 0
0x5	0b0101	SPI Slave Mode	CPOL = 0, CPHA = 1
0x6	0b0110	SPI Slave Mode	CPOL = 1, CPHA = 0
0x7	0b0111	SPI Slave Mode	CPOL = 1, CPHA = 1
0xC	0b1100	JTAG	

* Modes not mentioned in the list may not be selected and lead to a malfunction of the device.

FPGA reset depends on different conditions:

- The user can press button SW2 to trigger FPGA reset.
- After power-on, all DC-DC converters must notify 'power good' to finish reset state.
- The host controller can trigger reset via SPI or JTAG interface. In this case either level shifter U13 or U14 will feed the host's reset signal to the GateMate^{TM} FPGA.
- An external SPI device can feed a reset signal to the FPGA via the SPI connector J3 pin 9 (see Figure 3.8).
- An external JTAG device can feed a reset signal to the FPGA via the JTAG connector J4 pin 5 (see Figure 3.9).
- The user application can trigger FPGA reset via GPIO bank connector J-C pin 41 (APP_RESET_OUT). This signal can be disabled via Jumper JP10.

The GPIO bank connector feeds a reset signal APP_RESET_IN to the user application. This is either the reset button SW2 or any reset condition mentioned above (see Figure 3.10).

Every GPIO bank connector has a APP_RESET_OUT signal. These are all connected together and are called 'User application reset out' in Figure 3.10.

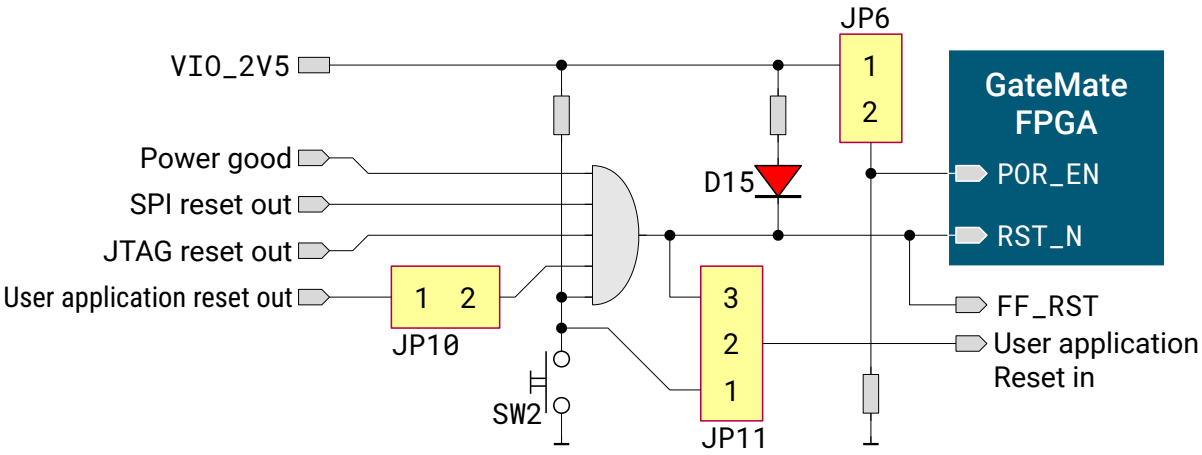

Figure 3.10: *Reset module*

After configuration, the GateMate™ FPGA reports whether the data stream was successfully loaded or not.

- LED D10 (green) is switched on when the data stream has completely been transferred.
- LED D9 (red) is switched on when an error occured.

Both signals are also passed to the host controller as shown in Figures 3.11 and 3.12. In case of a failed loading, reset should be triggered in order to load the data stream again.

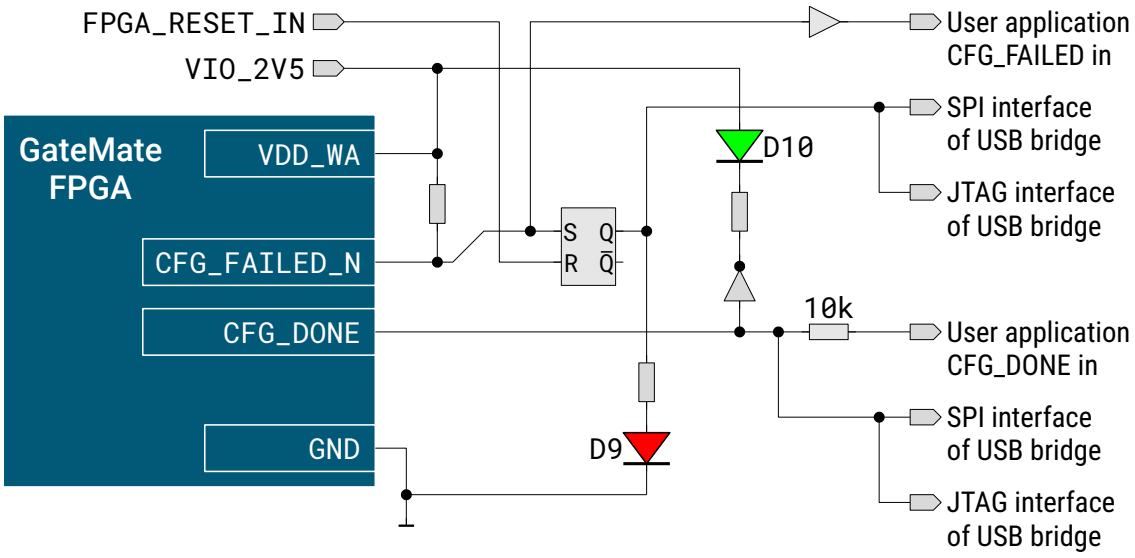

Figure 3.11: *Configuration status signals on evaluation board version 3.1*

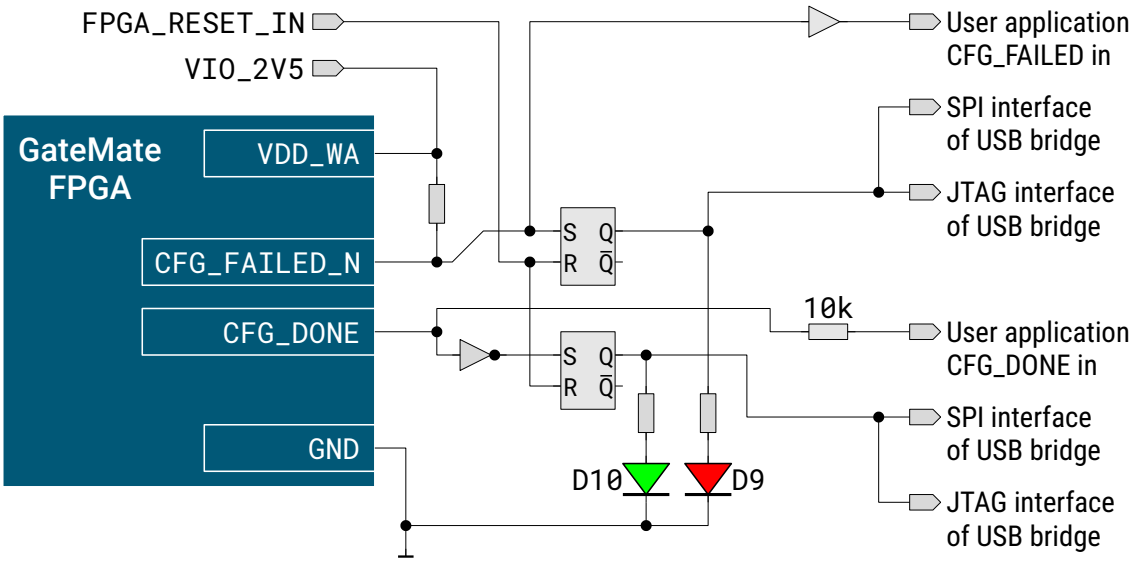

Figure 3.12: *Configuration status signals on evaluation board version 3.2*

3.5 Clock Generation and Distribution

The evaluation board has an on-board oscillator X1 with 10.000 MHz frequency. This signal is connected to GPIO IO_SB_A8 which is the input for clock 0 (see Figure 3.13). The oscillator can be disabled with jumper JP8.

The GateMate™ FPGA has three more clock inputs connected to the GPIO WA bank. The evaluation board has these clocks prepared for usage, but some components have to be populated by the user as shown in Figure 3.15.

Clock 1: Another oscillator can be populated or an external clock source can be used via SMA jack J8.

Clock 2 and 3: The user application can feed two clock signals to the FPGA inputs. Jumpers JP1 and JP2 must be populated to select the clock source.

Finally, a low-voltage differential signaling (LVDS) clock oscillator can be populated to generate a serializer / deserializer (SerDes) input clock as shown in Figure 3.14. Please note, that also series resistors R73 and R74 have to be populated (see Figure 3.19 on page 39).

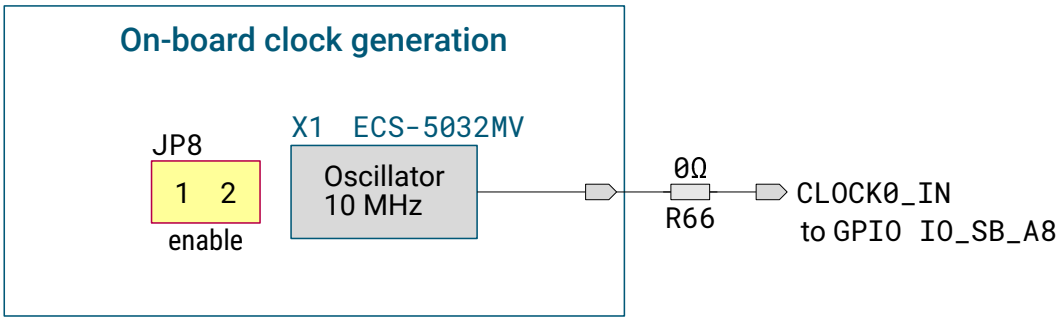

Figure 3.13: 10 MHz *on-board clock oscillator*

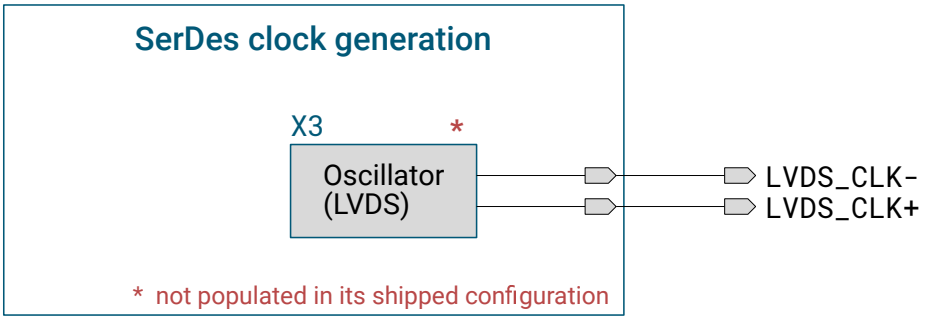

Figure 3.14: *Optional SerDes clock (LVDS clock oscillator)*

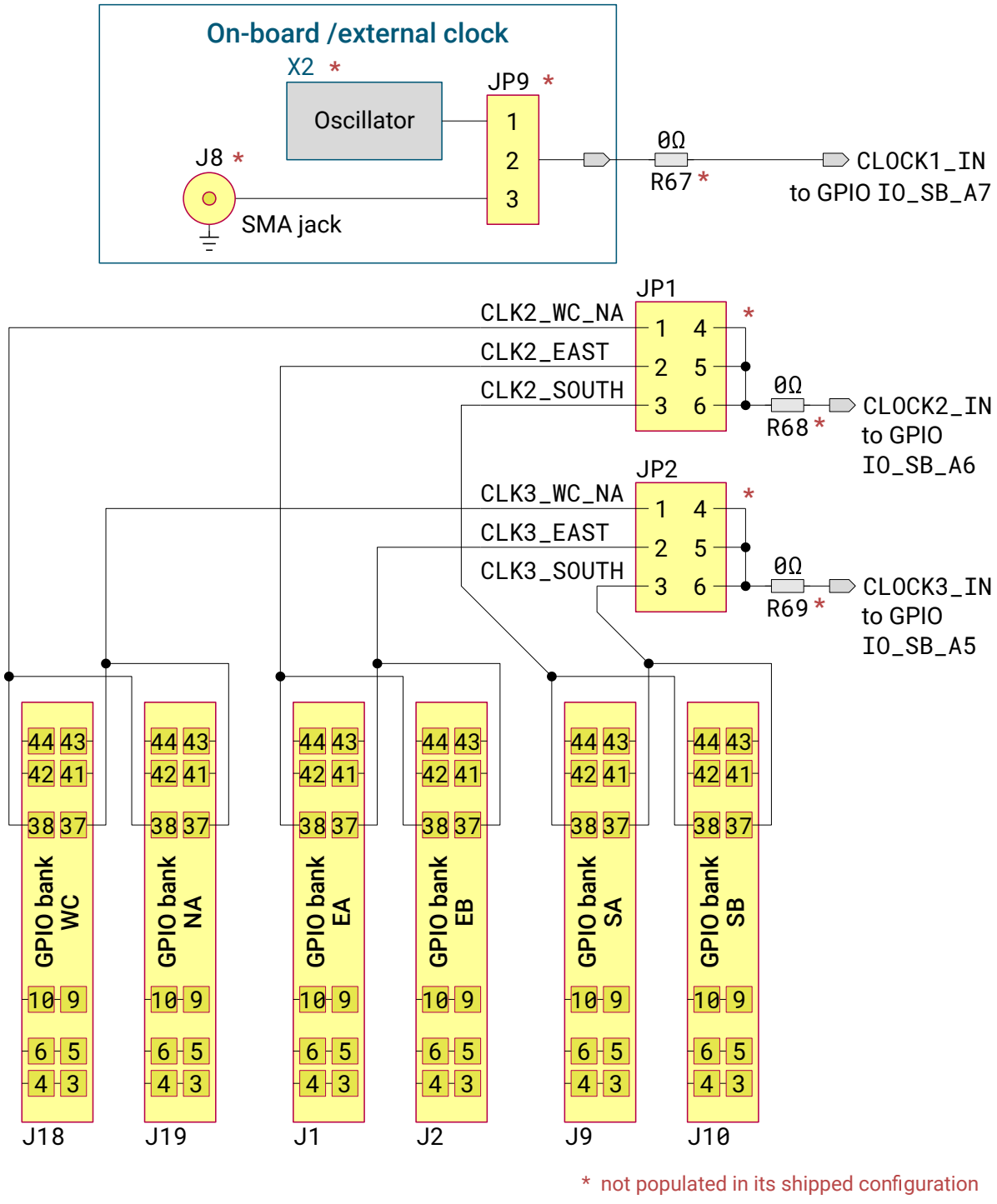

Figure 3.15: *Optional clock signals*

3.6 GPIO Connection to the User Application

The user application can be connected to one or more GPIO banks. Up to 6 banks are available. The other GPIO banks are assigned elsewhere.

All GPIO bank connectors have the same pinout as shown in Figure 3.16. Please note, that the GPIOs are arranged in two different ways with overturned signal vector. This is done to allow free choice of a GPIO bank for 1-bank user applications as shown in Figure 2.3 on page 17 and differential signal routing on the evaluation board at the same time. The PCB routing of all GPIO signals of banks EA and EB are inter-pair as well as intra-pair length matched. Details to the routing length are given in Table 3.8.

The user application can get it's power supply from the 3.3 V on-board DC-DC converter. In addition, GPIO voltage can be feed from the evaluation board to the user application or vice versa. Table 3.7 explains these VIOin and VIOout supply lines. The overall list of the GPIO bank connectors J-C is given in Table 3.6.

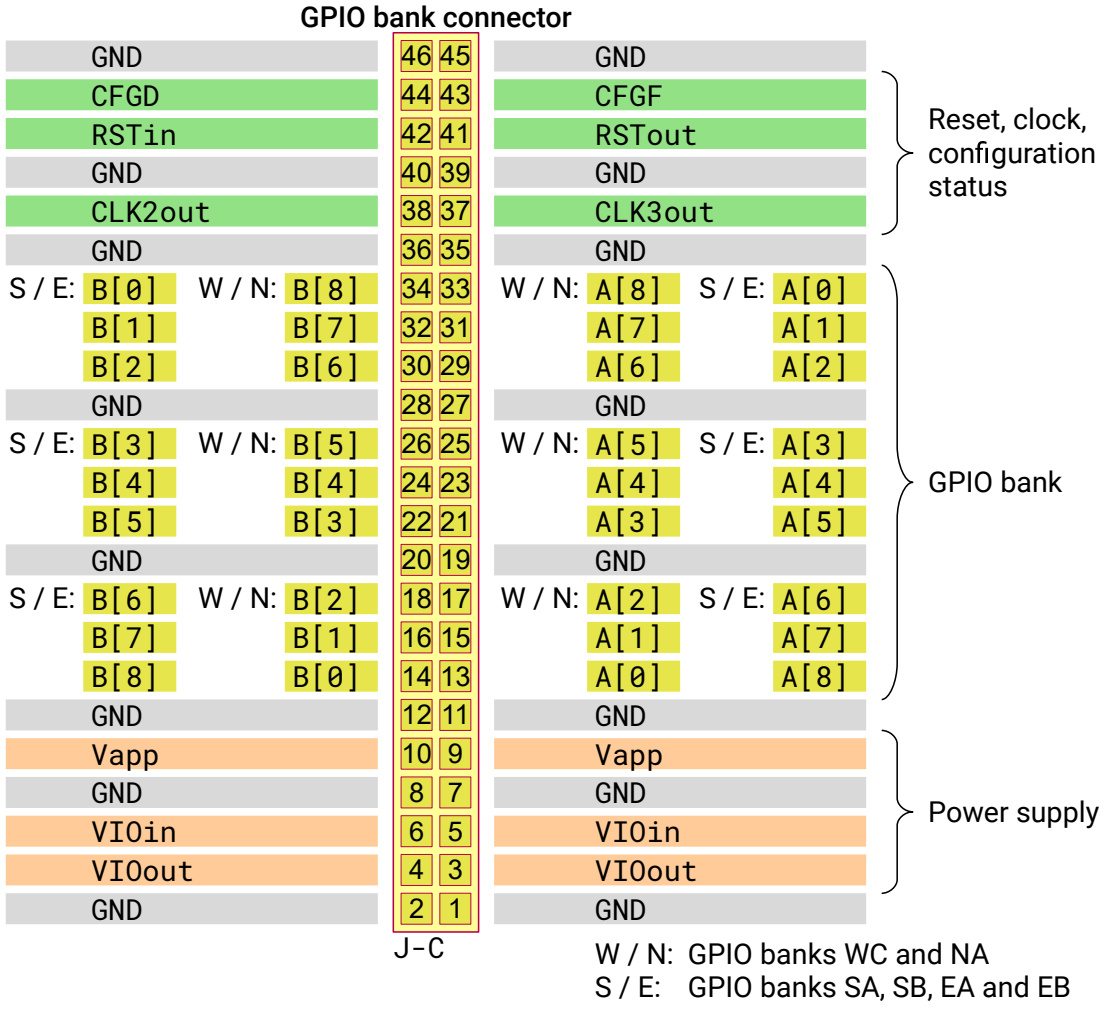

Figure 3.16: *GPIO bank connector J-C*

Table 3.6: *Pin assignment of GPIO connector J-C*

J-C pin	J-C signal	Schematic signal	Funktion
3 , 4	VIOout		see Table 3.7
5 , 6	VIOin		see Table 3.7
9 , 10	Vapp	VDD_APP	VIO_3V3 from power module
13 .. 33 [1]	A[8:0] or vice versa		to / from FPGA GPIO bank
14 .. 34 [2]	B[8:0] or vice versa		dto.
37	CLK3out		• 3 different signal pairs WC & NA, SA & SB and EA & EB from J-C connectors • to clock distribution jumper block JP2
38	CLK2out		• dto. • to clock distribution jumper block JP1
41	RSTout	APP_RESET_OUT	• from 6 GPIO connectors J-C • to reset circuitry via JP10
42	RSTin	APP_RESET_IN	• from JP11 of reset circuitry • to 6 GPIO connectors J-C
43	CFGF	3.1: CFG_FAILED_APP 3.2: /CFG_FAILED_APP [3]	• from FPGA pin CFG_FAILED_N • to 6 GPIO connectors J-C and FTDI chip (latched with flip-flop) via bus transceiver
44	CFGD	CFG_DONE_APP	• from FPGA pin CFG_DONE • to 6 GPIO connectors J-C and FTDI chip via bus transceiver • latched with flip-flop for PCB version 3.2

[1] odd only, pins 19 and 27 are GND
[2] even only, pins 20 and 28 are GND
[3] signal name depends on PCB version

Table 3.7: *Power input and output of GPIO connector J-C in Figures 3.4, 3.5 and 3.6 (pages 24 to 26)*

J-C	GPIO bank	VIOin	VIOout
J1	EA	from JP3 (selection)	to JP5, supply option for FPGA GPIO banks
J2	EB	dto.	dto.
J9	SA	VIO_2V5 from power module	not connected
J10	SB	dto.	dto.
J18	WC	from JP15 (selection)	to JP16, supply option for FPGA GPIO banks
J19	NA	dto.	dto.

Table 3.8: *Maximum intra-pair and inter-pair length mismatch of the GPIO banks*

	GPIO bank	Intra-pair length mismatch	Inter-pair length mismatch
Values for board version 3.1	EA *	0.9 mm	2.0 mm
	EB *	1.8 mm	1.8 mm
	SA	3.4 mm	11.7 mm
	SB	3.6 mm	13.0 mm
	NA	4.9 mm	12.1 mm
	WC	5.3 mm	14.4 mm
Values for board version 3.2	EA *	1.6 mm	2.1 mm
	EB *	0.1 mm	0.2 mm
	SA	0.4 mm	8.7 mm
	SB	0.5 mm	9.4 mm
	NA	0.6 mm	7.2 mm
	WC	0.6 mm	9.6 mm

* Best fit. Recommended for high speed applications.

3.7 Pmod Interface

GPIO bank NB constitudes a Pmod interface with two standard 12-pin connectors J17A and J17B.

Supply voltage 3.3 V should be selected via jumper JP14 to fulfill Pmod specification. If desired for certain applications, 2.5 V supply can be choosen exceptionally. Please note, that many Pmod devices will not work properly in this case.

Table 3.9 shows the GPIO signals connected to the Pmod interface connectors J17A and J17B.

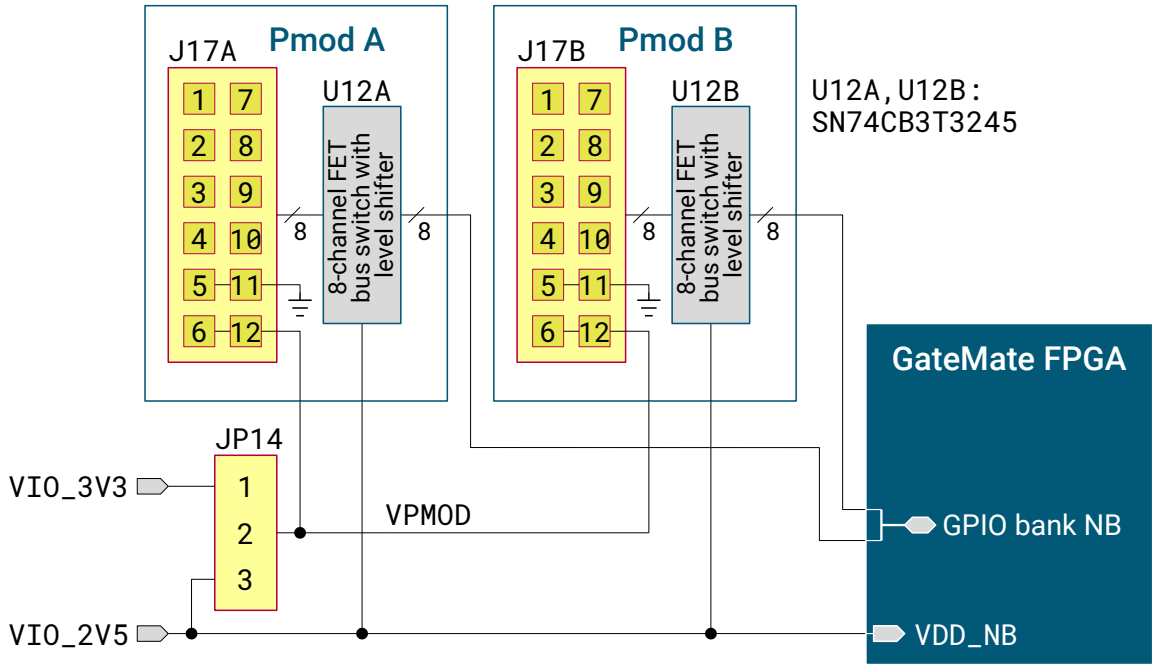

Figure 3.17: *GPIO bank NB with Pmod interface*

Table 3.9: *Pmod signal assignment of J17A and J17B connectors*

J17A/B pin	Pmod signal	GPIO for Pmod A	GPIO for Pmod B	J17A/B pin	Pmod signal	GPIO for Pmod A	GPIO for Pmod B
1	IO1	IO_NB_A0	IO_NB_A4	7	IO5	IO_NB_B0	IO_NB_B4
2	IO2	IO_NB_A1	IO_NB_A5	8	IO6	IO_NB_B1	IO_NB_B5
3	IO3	IO_NB_A2	IO_NB_A6	9	IO7	IO_NB_B2	IO_NB_B6
4	IO4	IO_NB_A3	IO_NB_A7	10	IO8	IO_NB_B3	IO_NB_B7
5	GND			11	GND		
6	VPMOD			12	VPMOD		

(Signal assignment due to Digilent Pmod Interface Specification 1.2.0, type 1A, expanded GPIO)

3.8 HyperRAM Device

GPIO bank WB is used to provide an on-board HyperRAM memory (see Figure 3.18). U10 is a 64 Mb device which is connected to the GPIO bank as shown in Table 3.10.

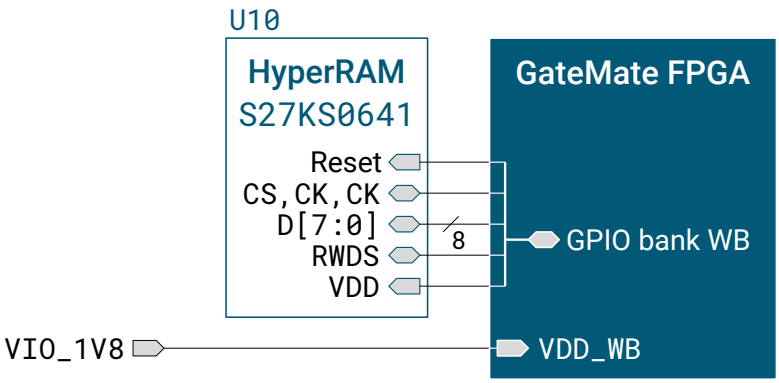

Figure 3.18: *GPIO bank WB with HyperRAM device*

Table 3.10: *GPIO assignment to the on-board HyperRAM device*

GPIO	HyperRAM signal	GPIO	HyperRAM signal
IO_WB_A0	–	IO_WB_B0	$\overline{\text{CS}}$
IO_WB_A1	–	IO_WB_B1	–
IO_WB_A2	$\overline{\text{RESET}}$	IO_WB_B2	–
IO_WB_A3	CK	IO_WB_B3	$\overline{\text{CK}}$
IO_WB_A4	–	IO_WB_B4	RWDS
IO_WB_A5	DQ0	IO_WB_B5	DQ1
IO_WB_A6	DQ2	IO_WB_B6	DQ3
IO_WB_A7	DQ4	IO_WB_B7	DQ5
IO_WB_A8	DQ6	IO_WB_B8	DQ7

3.9 SerDes Interface

The evaluation board is prepared to offer a SerDes interface. Figure 3.19 shows, that the SMA jacks J13 . . J16 must be populated from the user to get access to the CCGM1A1 SerDes interface.

There are two ways to feed in the SerDes clock signal:

1. SMA jacks J11 and J12 are populated to feed in an external LVDS clock.
2. An on-board LVDS oscillator and the series resistors R73 and R74 are populated (see also Figure 3.14 on page 32).

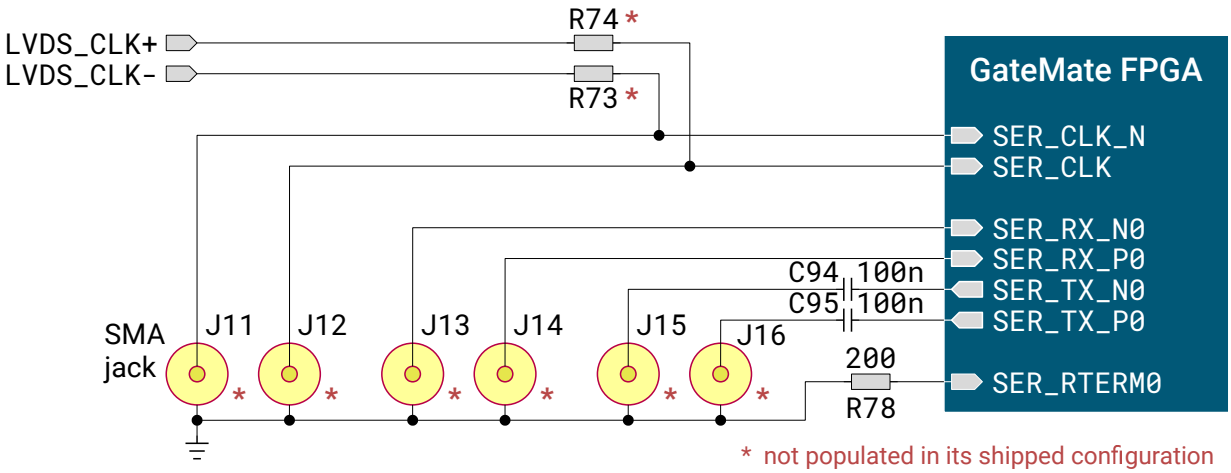

Figure 3.19: *Optional SerDes interface*

Chapter 4

Electrical Characteristics

Table 4.1: *Absolute maximum characteristics of the GateMate™ FPGA Evaluation Board*

Symbol	Min	Typ	Max	Unit	Description
	−40		125	°C	Junction temperature
V_{in}	−0.3		6.5	V	Power supply from J5 or J6
V_{in}	−0.3		6.0	V	Power supply from J7
T_{stg}	−55		150	°C	Storage temperature

Table 4.2: *Operating characteristics of the GateMate™ FPGA Evaluation Board*

Symbol	Min	Typ	Max	Unit	Description
	−40		85	°C	Operating temperature
V_{in}	4.0		6.0	V	Power supply from J5 or J6
V_{in}	4.75		5.75	V	Power supply from J7
I_{in}		140		mA	Power consumption during reset

Table 4.3: *GPIO characteristics in single-ended mode*

Symbol	Min	Typ	Max	Unit	Description
VDD_{IO}	1.1		2.7	V	I/O supply voltage (GPIO banks and VDD_CLK)
V_{IN}	−0.4		$VDD_{IO} + 0.4$	V	Input voltage range
Schmitt-trigger function disabled:					
V_{IH}	0.43		0.51	VDD_{IO}	Input high threshold voltage
V_{IL}	0.45		0.51	VDD_{IO}	Input low threshold voltage
V_{HYST}		0		V	Hysteresis
Schmitt-trigger function enabled:					
V_{IH}	0.61		0.67	VDD_{IO}	Input high threshold voltage
V_{IL}	0.31		0.39	VDD_{IO}	Input low threshold voltage
V_{HYST}	0.26		0.33	VDD_{IO}	Hysteresis
Output driver disabled:					
I_{IL}			1	µA	Input pin current when driven active low
I_{IH}			1	µA	Input pin current when driven active high
R_{PU}		50		kΩ	Pull-up resistance
R_{PD}		50		kΩ	Pull-down resistance
$I_{DD,max}$			158	µA	Maximum supply current at GPIO input at transition point

Table 4.4: *GPIO characteristics in LVDS mode*

Symbol	Min	Typ	Max	Unit	Description
VDD_{IO}	1.62		2.75	V	I/O supply voltage
I_{out}		3.2		mA	Output current when LVDS output current boost is set to nominal current
I_{out}		6.4		mA	Output current when LVDS output current boost is set to increased output current
VCM_{TX}		$VDD_{IO}/2$		V	Common-mode voltage
R_{term}	90	100	130	Ω	

Acronyms

FPGA	field-programmable gate array	16
GPIO	general purpose input / output	5–7, 12, 16, 18, 24, 26, 29, 32, 34, 37, 38, 41
JTAG	Joint Test Action Group	5, 12, 16, 27–29
LVDS	low-voltage differential signaling	6, 7, 32, 39, 41
PCB	printed circuit board	5, 12, 16, 18, 21, 34
Pmod	pheripheral module interface (Digilent)	6, 7, 12, 24, 37
SerDes	serializer / deserializer	6, 12, 32, 39
SPI	Serial Peripheral Interface	5, 12, 16, 27, 29
USB	Universal Serial Bus	12, 16, 21, 22

GateMate™ FPGA
Evaluation Board Datasheet
Generic Evaluation Board for GateMate
DS1003
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Cologne Chip