GateMate™ FPGA Programmer Datasheet

Programmer Version 1.3 Schematics

DS1002

Datasheet August 2023

Cologne Chip AG
Eintrachtstr. 113
50668 Köln

Tel.: +49 (0) 221 / 91 24-0
Fax: +49 (0) 221 / 91 24-100

https://colognechip.com
info@colognechip.com

Copyright 2019 - 2023 Cologne Chip AG

All Rights Reserved

The information presented can not be considered as assured characteristics. Data can change without notice. Parts of the information presented may be protected by patent or other rights. Cologne Chip products are not designed, intended, or authorized for use in any application intended to support or sustain life, or for any other application in which the failure of the Cologne Chip product could create a situation where personal injury or death may occur.

Contents

About this Document 5

1 Mechanical Dimensions 7

2 PCB components 9

3 Programmer Schematics 11

4 Bill of Materials 15

About this Document

This is a sub-document in an ensemble of GateMate™ FPGA Programmer documents, which include the following documents:

- **DS1002** – GateMate™ FPGA Programmer Datasheet
- **DS1002** – GateMate™ FPGA Programmer Version 1.4 Schematics

All documents of the programmer are always updated together. Please make sure that you use these documents with the same date.

The change history of the complete document ensemble can be found in the main document.

For more information please refer to the following documents:

- Technology Brief of GateMate™ FPGA
- **DS1001** – GateMate™ FPGA CCGM1A1 Datasheet
- **UG1002** – GateMate™ FPGA Toolchain Installation User Guide

Cologne Chip provides a comprehensive technical support. Please visit our website for more information or contact our support team.

Chapter 1

Mechanical Dimensions

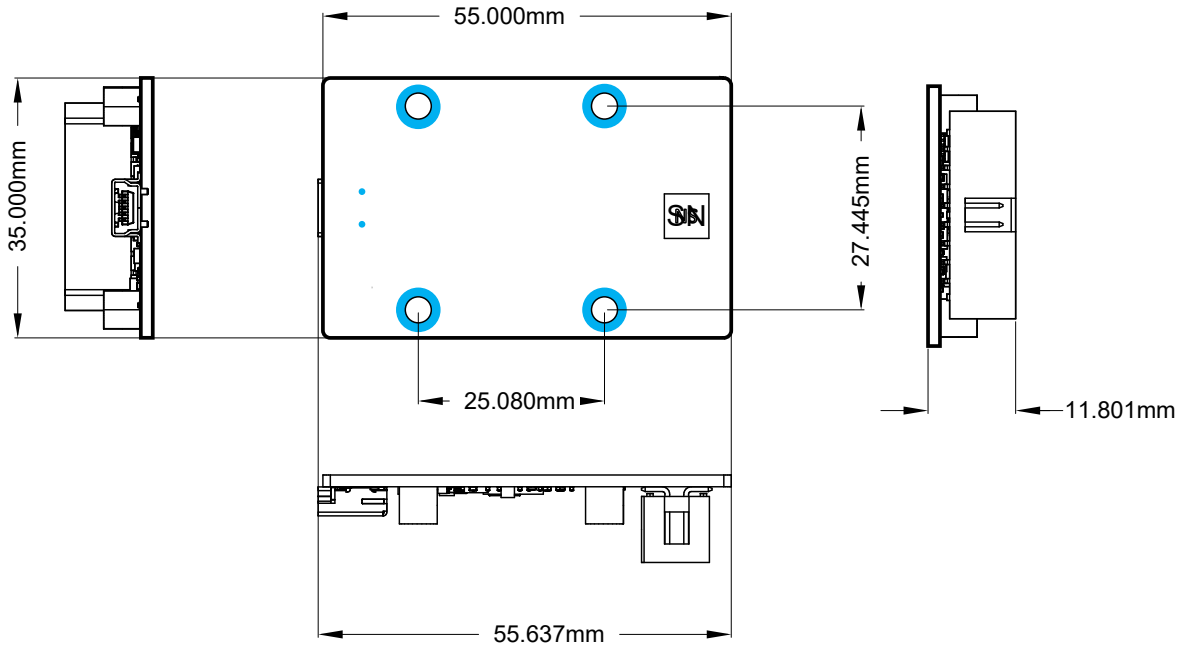


Figure 1.1: *Mechanical dimensions of the GateMate™ FPGA Programmer 1.3 (top side)*

Chapter 2

PCB components

The location of the main components can be found in Figure 2.1. Table 2.1 gives a short specification of these components. For more details, please see the schematics in Section 3.

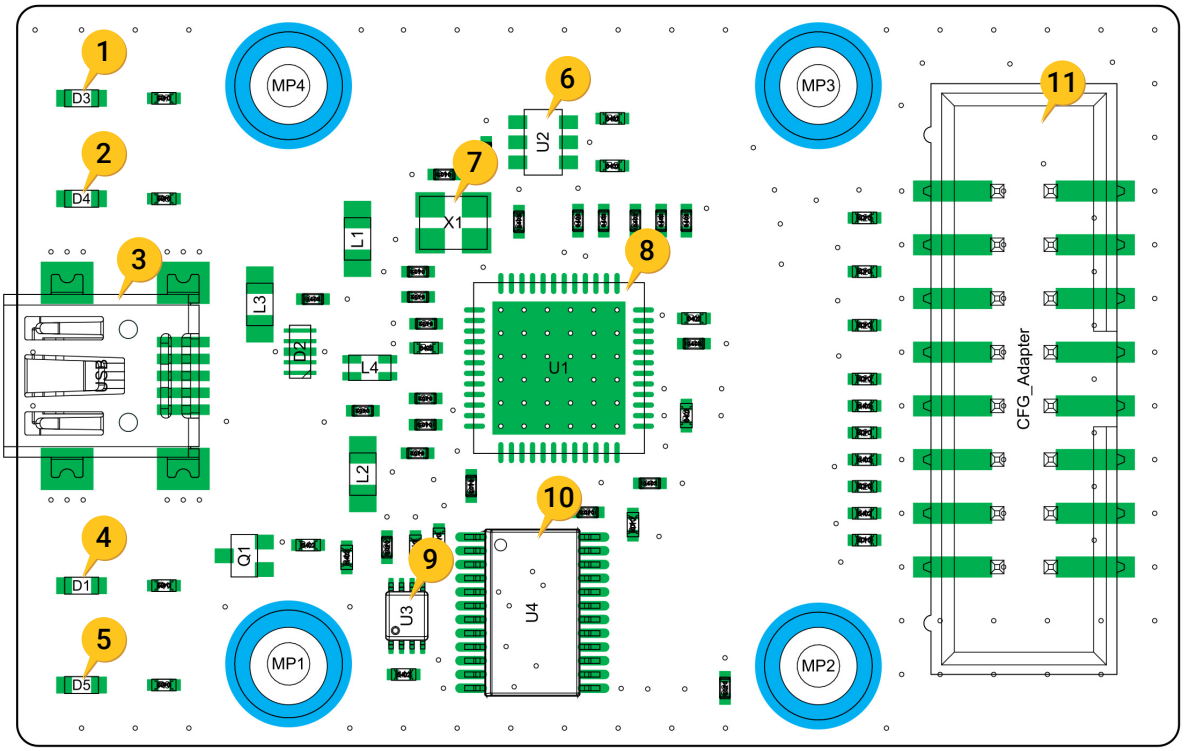


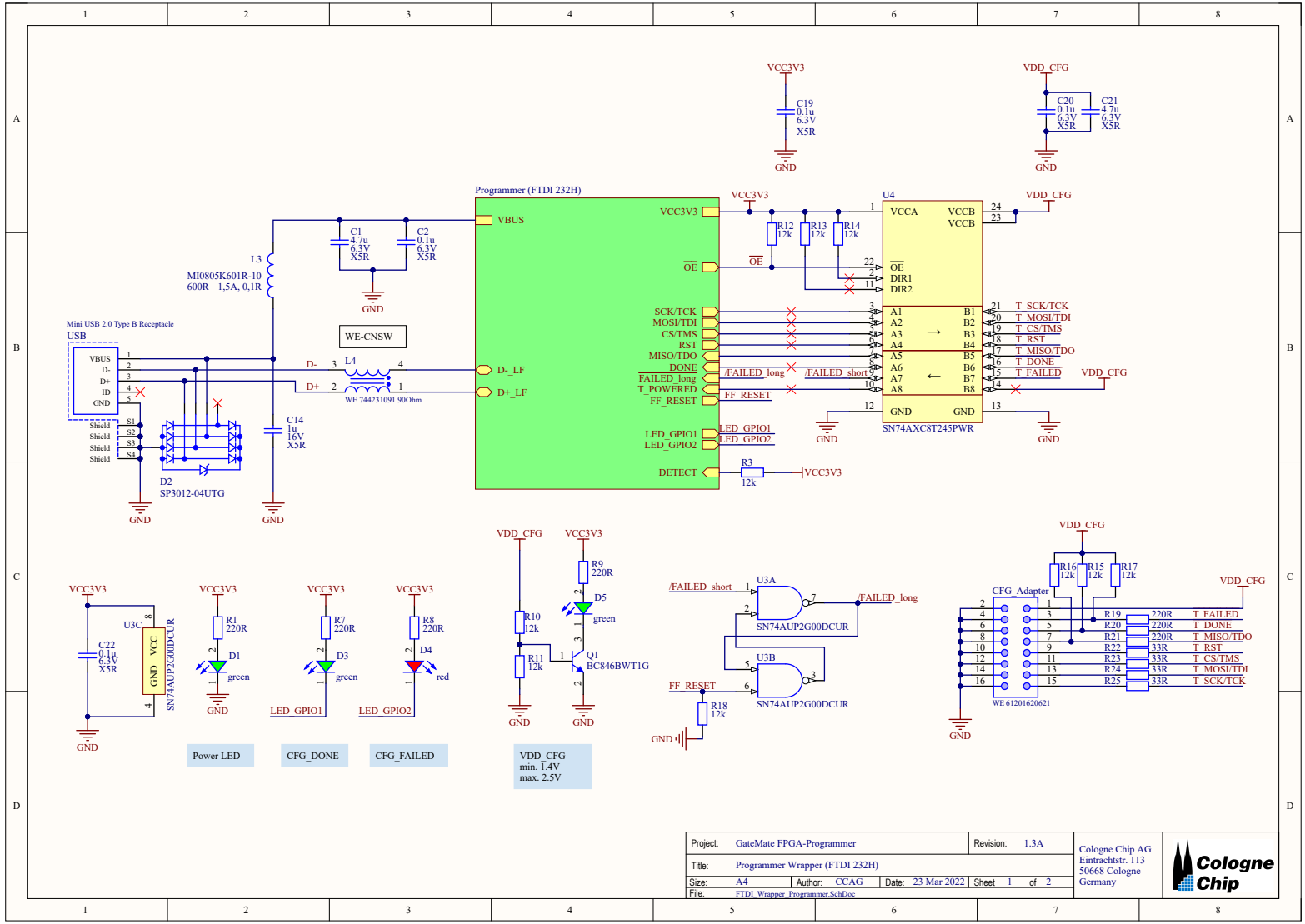
Figure 2.1: *Main components of the GateMate^{TM} FPGA Programmer 1.3 (top side)*

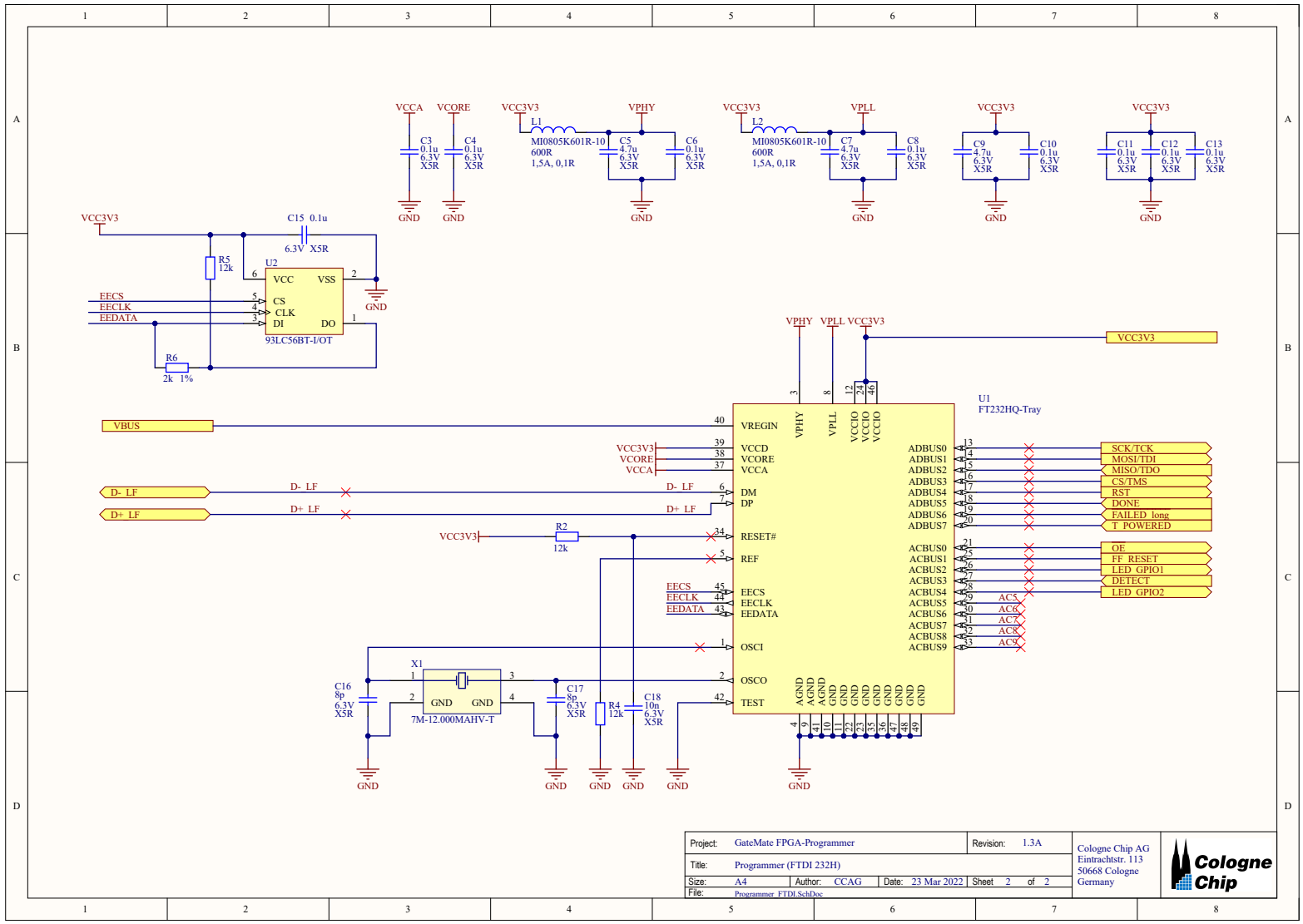
Table 2.1: *Main components of the GateMate^{TM} FPGA Programmer 1.3 (top side)*

Number	Designator	Component
1	D3	Status LED `CFG_DONE` (from USB bridge)
2	D4	Status LED `CFG_FAILED_N` (from USB bridge)
3	USB	Mini USB 2.0 Type B Receptacle
4	D1	Status LED for power from USB host
5	D5	Status LED for GPIO power from CFG_Adapter
6	U2	Microchip 93LC56BT-I/OT, 2 Kbit 128×16, 2.5 V, FTDI configuration EEPROM
7	X1	Oscillator 12.000 MHz ±30ppm, 8 pF
8	U1	Microchip FTDI FT232HQ-Tray
9	U3	Microchip SN74AUP2G00DCUR, failed detection latch
10	U4	Microchip SN74AXC8T245PWR, bus transceiver U1 / CFG_Adapter
11	CFG_Adapter	Male box header, pitch 2.54 mm, 2×8 pins

Chapter 3

Programmer Schematics


Programmer (FTDI 232H)
VBUS
VCC3V3
OE
SCK/TCK
MOSI/TDI
CS/TMS
RST
MISO/TDO
DONE
FAILED_long
T_POWERED
FF_RESET
LED_GPIO1
LED_GPIO2
DETECT
D-_LF
D+_LF
U4
SN74AXC8T245PWR
VCCA
VCCB
DIR1
DIR2
A1
A2
A3
A4
A5
A6
A7
A8
B1
B2
B3
B4
B5
B6
B7
B8
GND
T_SCK/TCK
T_MOSI/TDI
T_CS/TMS
T_RST
T_MISO/TDO
T_DONE
T_FAILED
/FAILED_long
/FAILED_short
VDD_CFG
Mini USB 2.0 Type B Receptacle
USB
VBUS
D-
D+
ID
GND
Shield
D2
SP3012-04UTG
WE-CNSW
L3
MI0805K601R-10
600R 1,5A, 0,1R
L4
WE 744231091 90Ohm
C1
4.7u
6.3V
X5R
C2
0.1u
6.3V
X5R
C14
1u
16V
X5R
C19
0.1u
6.3V
X5R
C20
0.1u
6.3V
X5R
C21
4.7u
6.3V
X5R
R12
12k
R13
12k
R14
12k
R3
12k
U3A
U3B
U3C
SN74AUP2G00DCUR
R18
12k
R9
220R
D5
green
Q1
BC846BWT1G
R10
12k
R11
12k
R1
220R
D1
green
R7
220R
D3
green
R8
220R
D4
red
C22
0.1u
6.3V
X5R
Power LED
CFG_DONE
CFG_FAILED
VDD_CFG
min. 1.4V
max. 2.5V
CFG_Adapter
WE 61201620621
R16
12k
R15
12k
R17
12k
R19
R20
R21
R22
R23
R24
R25
220R
33R
Project: GateMate FPGA-Programmer
Revision: 1.3A
Title: Programmer Wrapper (FTDI 232H)
Size: A4
Author: CCAG
Date: 23 Mar 2022
Sheet 1 of 2
File: FTDI_Wrapper_Programmer.SchDoc
Cologne Chip AG
Eintrachtstr. 113
50668 Cologne
Germany


VCCA
VCORE
VCC3V3
VPHY
VPLL
L1
MI0805K601R-10
600R
1,5A, 0,1R
L2
C3 0.1u 6.3V X5R
C4 0.1u 6.3V X5R
C5 4.7u 6.3V X5R
C6 0.1u 6.3V X5R
C7 4.7u 6.3V X5R
C8 0.1u 6.3V X5R
C9 4.7u 6.3V X5R
C10 0.1u 6.3V X5R
C11 0.1u 6.3V X5R
C12 0.1u 6.3V X5R
C13 0.1u 6.3V X5R
GND
C15 0.1u 6.3V X5R
R5 12k
R6 2k 1%
U2
VCC
VSS
CS
CLK
DI
DO
93LC56BT-I/OT
EECS
EECLK
EEDATA
U1
FT232HQ-Tray
VREGIN
VCCD
VCORE
VCCA
DM
DP
RESET#
REF
EECS
EECLK
EEDATA
OSCI
OSCO
TEST
VCCIO
AGND
ADBUS0
ADBUS1
ADBUS2
ADBUS3
ADBUS4
ADBUS5
ADBUS6
ADBUS7
ACBUS0
ACBUS1
ACBUS2
ACBUS3
ACBUS4
ACBUS5
ACBUS6
ACBUS7
ACBUS8
ACBUS9
SCK/TCK
MOSI/TDI
MISO/TDO
CS/TMS
RST
DONE
FAILED_long
T_POWERED
OE
FF_RESET
LED_GPIO1
DETECT
LED_GPIO2
VBUS
D- LF
D+ LF
R2 12k
R4 12k
X1
7M-12.000MAHV-T
C16 8p 6.3V X5R
C17 8p 6.3V X5R
C18 10n 6.3V X5R
Project: GateMate FPGA-Programmer
Revision: 1.3A
Title: Programmer (FTDI 232H)
Size: A4
Author: CCAG
Date: 23 Mar 2022
Sheet 2 of 2
File: Programmer_FTDI.SchDoc
Cologne Chip AG
Eintrachtstr. 113
50668 Cologne
Germany
Cologne Chip

Chapter 4

Bill of Materials

Table 4.1: *Bill of Materials (sorted by designator)*

Component	Specification	Designators	Count
1u	16V X5R	C14	1
8p	6.3V X5R	C16, C17	2
10n	6.3V X5R	C18	1
4.7u	6.3V X5R	C1, C5, C7, C9, C21	5
0.1u	6.3V X5R	C2, C3, C4, C6, C8, C10, C11, C12, C13, C15, C19, C20, C22	13
WE-612 016 206 21	Box header vertical 2x8 pins 2.54 mm	Z2	1
SP3012-04UTG	TVS diode	D2	1
WE-150 060 RS7 322	LED red	D4	1
WE-150 060 VS7 322	LED green	D1, D3, D5	3
MI0805K601R-10	600R 1,5A, 0,1R	L1, L2, L3	3
WE-744 231 091	CNSW 370mA 90Ohm 100MHz	L4	1
BC846BWT1G		Q1	1
2k	1%	R6	1
12k	1%	R2, R3, R4, R5, R10, R11, R12, R13, R14, R15, R16, R17, R18	13
220R	1%	R1, R7, R8, R9, R19, R20, R21	7
33R	1%	R22, R23, R24, R25	4
FT232HQ-Tray		U1	1
93LC56BT-I/OT		U2	1

Continued on next page

Table 4.0: *Bill of Materials (sorted by designator)*

Continued from previous page

Component	Specification	Designators	Count
SN74AUP2G00DCUR		U3	1
SN74AXC8T245PWR		U4	1
WE-651 005 161 21	Mini USB 2.0 Type B Receptacle	Z4	1
7M-12.000MAHV-T		X1	1

GateMate™ FPGA
Programmer Datasheet
Programmer Version 1.3 Schematics
DS1002
August 2023

Cologne Chip