Cologne Chip

DIGICC™ PLL Technology

Technology Background

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1 Introduction

1.1 Motivation

Phase-locked loops (PLLs) are a widely needed and used circuitry in today's semiconductor chips. They are mainly used for three different tasks:

(1) Generation of high frequency on-chip clocks by frequency multiplication

(2) Reduction of clock skew

(3) Jitter attenuation

A PLL is characterized by the frequency range, jitter, jitter attenuation and lock time. PLLs of type (1) are only used for generation of high frequency stable clocks and are normally feed by quartz controlled oscillators so that there is no need for a jitter attenuation.

Unfortunately PLLs are mixed-mode circuitries up to now. They must combine analog parts as loop filter and VCO with digital parts as the frequency divider. So at least the analog circuitry must be adapted to every new CMOS process technology. For digital circuits the number of gates per square millimeter approximately doubles per chip generation. Integration of analog parts in newer deep submicron technologies is much more tough and additionally complicated because the usable voltage ranges decrease with every new integration step. So deep submicron technologies use core voltages below 2 V. Furthermore, some area is needed to realize accurate parameters.

If it were possible to realize a PLL as 'pure' digital circuit, no effort would be needed to scale the device for ever new CMOS process technology – and furthermore, the full integration advantage of a digital circuit would be feasible. No special silicon process and test technology known as 'mixed-mode' would be needed as well.

1.2 Overview

The goal of the new DIGICC^{TM} PLL technology is that all components of a high performance PLL are really full digital. There are neither external components as loop capacitors nor special I/O, GND or VDD pins. There is even no need for a special location for the PLL core on the die.

1.3 Patents

Several patents were granted in different countries of the world for the DIGICC^{TM} technology. Please contact Cologne Chip for special information or for license requests.

2 Pure digital PLL

2.1 Traditional PLL

Traditional PLLs are composed of a voltage controlled oscillator (VCO) whose output frequency is controlled by an input voltage. The VCO output f_{out} is devided by an integer value to get a frequency f_{cmp} which is compared to the input frequency f_{in}. The objective is to generate an output frequency so that $f_{out} = N \cdot f_{in}$.

The output signal of the phase & frequency comparator is converted into a voltage by the loop filter. This is normally a simple low pass filter. Figure 1 shows a block diagram of a traditional PLL.

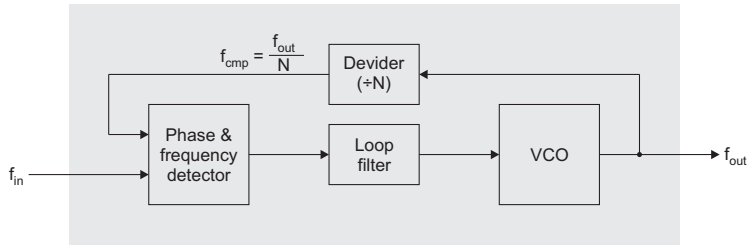

Figure 1: *Standard PLL structure*

The jitter of the output frequency f_{out} is a composition of several jitter sources. There are random jitter, jitter introduced by noise on the voltage control input of the VCO, adjust voltage pulses coming through the loop filter and supply voltage noise.

The lock time of a PLL is defined as the time which elapses from initial or reset condition up to the phase-locked condition of the output frequency. It is mainly influenced by the phase comparator, the loop filter and the tolerable output jitter.

2.2 Digital PLL approach

The digital PLL approach uses pure digital functional blocks instead of their analog counterparts as shown in Figure 2. The output frequency is generated from a digital controlled oscillator (DCO). The input frequency f_{in} and the frequency $f_{cmp} = f_{out}/N$ are compared and the phase and frequency difference lead to a counter control signal. The counter value, finally, drives the frequency selection of the DCO. This is only a rough description of the digital PLL approach. A more detailed explanation is given in the following sections.

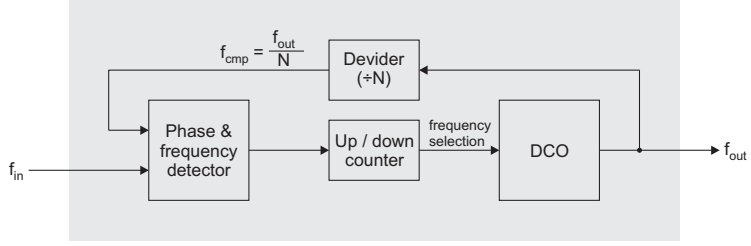

Figure 2: *Digital PLL approach*

2.3 Digital controlled oscillator (DCO)

The digital controlled oscillator uses a delay chain for the clock generation as shown in Figure 3. The chain length is a function of *k*. The gate delays are used to control the output frequency f_{out}. In the locked state of the PLL, the frequency selection value *k* is constant and two different frequencies $f(k)$ and $f(k+1)$ can be generated due to the value of *p*.

The minimum pulse delay t_0 depends on the CMOS technology.

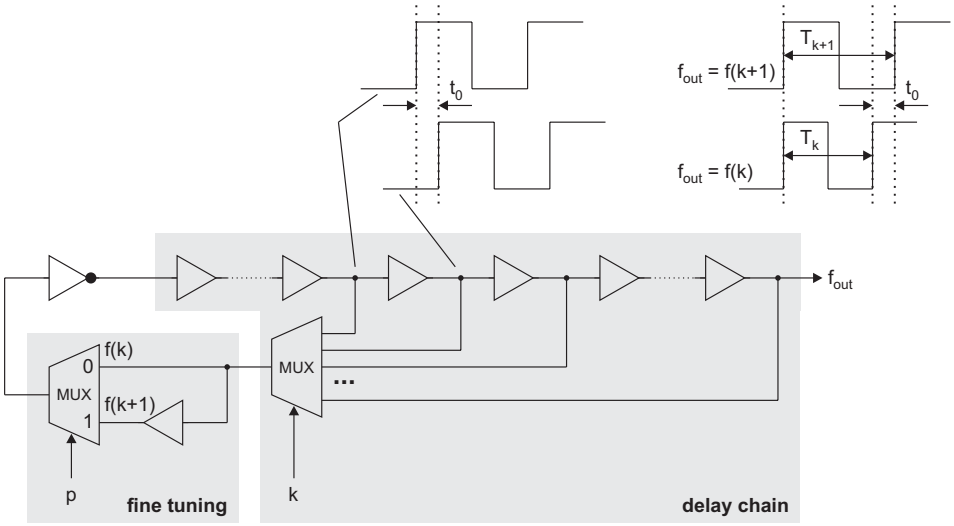

Figure 3: *Digital controlled oscillator*

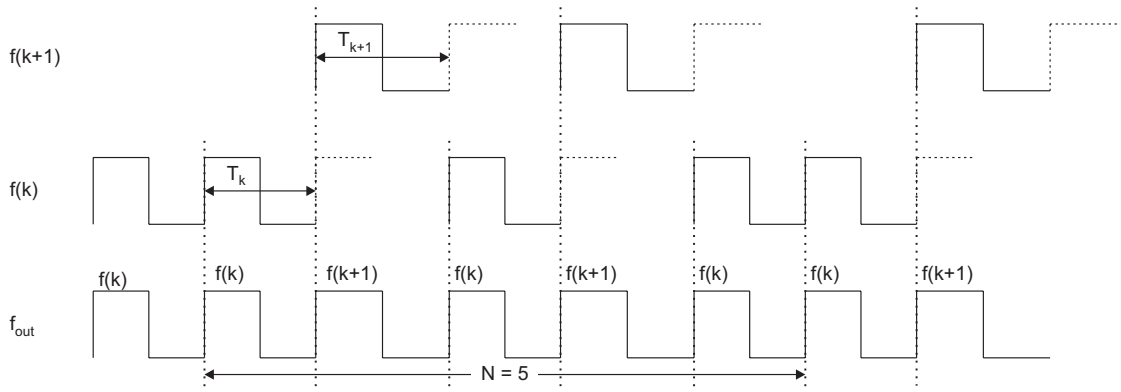

Figure 4: *Frequency f_{out} composition by pulses of two different frequencies $f(k)$ and $f(k+1)$*

The DCO has a fine tuning capability, which allows to generate *N* different frequencies in the range $f(k+1)..f(k)$ by ongoing switching between $f(k)$ (when $p=0$) and $f(k+1)$ (when $p=1$). Figure 4 shows an example with $N=5$.

$f(k)$ and $f(k+1)$ have constant period length $T(k)$ and $T(k+1)$ each. f_{out} consists of pulses with both $T(k)$ and $T(k+1)$ length. The maximum clock-to-clock jitter is

$$t_0 = T(k+1) - T(k) \quad .$$

f_{out} edges have a small jitter around the nominal edges which is never greater than t_0.

2.4 Phase & frequency detector

The phase & frequency detector compares $f_{cmp} = f_{out}/N$ with the reference frequency f_{in}. The detector output signal is used to control an up / down counter with 'count ± 1' or 'count ± 2' commands.

Because there are no analog components in the DIGICC™ PLL, it is not possible to measure the phase difference between f_{cmp} and f_{in}. The phase transition is detected instead, and due to the result the frequency of the DCO is slightly adjusted in a way that there must be a phase transition in the opposite direction. Thus there is a tiny phase oscillation around the exact output frequency. The frequency of the oscillator is adjusted when there is a better center frequency for this oscillation. This is done to compensate changes of temperature and supply voltage.

2.5 Up / down counter

The up / down counter consists of two parts. The output value of the lower part is used for fine tuning. The upper part delivers k to the DCO for frequency selection. Figure 5 shows a detailed structure of the digital PLL.

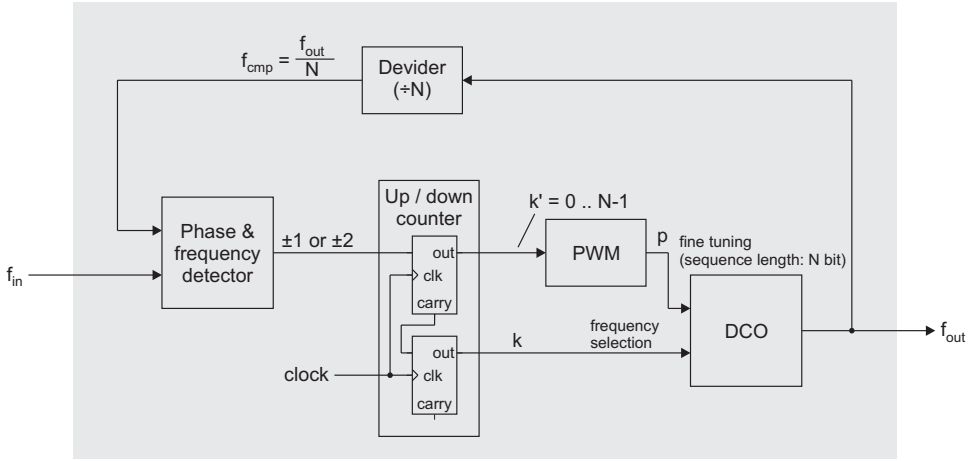

Figure 5: *Detailed structure of the digital PLL*

A pulse width modulator (PWM) gets the counter output k'. This value is converted into a N-bit sequence p which is used to generate pulses with $T(k)$ (when $p = 0$) or $T(k+1)$ (when $p = 1$) width as described in section 2.3.

The switching between the two frequencies can be optimized so that the overall jitter is minimized. This is done by switching just when the phase of the output frequency overtake or undertake the ideal phase of the output frequency. This is identical to a switching in the shortest possible distances. The PWM generates a programmable number of '1's in a period of N clocks and furthermore distributes the '1's in a way that the mean gap between two '1's is minimized. So all frequencies between $f(k+1)$ and $f(k)$ can be generated depending of the range of the PLL. Fortunately the introduced clock-to-clock jitter t_0 is also the maximum clock-to-clock jitter.

3 PLL parameters

3.1 Jitter scaling

For many PLL applications it is not the best solution to reduce the output jitter to the smallest possible value. This is due to the fact that problems known as EMI increase if the power spectrum is just concentrated at a very small frequency range.

EMI problems can easily be reduced with the digital PLL approach by a defined increase in jitter. This is widely acceptable for the clocking of processor systems.

The larger the smallest frequency increment is, the larger the jitter will be.

3.2 Lock time

The lock time of the DIGICC™ PLL is shorter than the typical lock time of analog PLLs. Analog loop filters need more time for a comparable jitter performance.

Another advantage of the digital PLL is the possibility to freeze the current (locked) state. This feature conserves the current settings for the output frequency f_{out} and needs nearly no lock time after the DCO oscillator has been enabled again. There might be just a small re-synchronization due to temperature drift or a slightly power supply change.

4 Implementation example as high speed PLL in an FPGA

The DIGICC™ PLL technology was implemented in different VIRTEX™ type FPGAs from XILINX. Measurement results are shown in Table 1. Due to the implementation in CLBs instead of real gates the performance of the PLL is decreased.

Table 1: *Measurement results of an FPGA implementation*

Measured variable	Result
PLL output frequency f_{out}	125 MHz
Reference frequency f_{in}	5 MHz
Typical clock-to-clock jitter	±270 ps (Sigma 150 ps)
Worst case clock-to-clock jitter	±490 ps (Sigma 190 ps)
Clock-to-clock jitter from supply voltage	1.2 ps/mV

5 Conclusion

DIGICC™ is a highly sophisticated new approach for a wide range of PLLs. It meets mixed mode requirements with a pure digital IP core.

No external components like additional power pads / pins, loop capacitors or others are needed. So a seamless integration in every new chip process technology is achieved and the scaling factor of a new digital chip generation can be fully exploited.

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